ARINC 429/575 Communications
AR1
Function Module

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	2/1/2018	ECO C05364, Initial release	SL
B	7/23/2019	- Reformatted to include numbers in headings. - Added register grouping headers in Register Description section and Function Register Map section. - Added Initiated BIT, Background Bit Threshold Programming registers and Summary Status	GC
B1	1/23/2020	- Added Firmware Revision and Release Dates for Pending functions	GC
B2	4/22/2020	- ECO C07519: Module manuals updated for formatting consistency. No technical or specification updates.	MC

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1 Introduction

This module manual provides information about the North Atlantic Industries, Inc. (NAI) ARINC 429/575 Communications Function Module: AR1. This module is compatible with all NAI Generation 5 motherboards.

ARINC 429/575 Communications Module AR1 provides ARINC 429 and 575 communications. ARINC 429 is a data transfer standard for aircraft avionics. It is an alternative to MIL-STD-1553. It uses a self-clocking, self-synchronizing data bus protocol (Tx and Rx are on separate ports). The physical connection wires are twisted pairs carrying balanced differential signaling. Data words are 32 bits in length and most messages consist of a single data word. Messages are transmitted at either 12.5 or 100 kbps to other system elements that monitor the bus messages. The transmitter constantly transmits either 32-bit data words or the NULL state. A single-wire pair is limited to one transmitter and no more than 20 receivers. The protocol allows for self-clocking at the receiver end, thus eliminating the need to transmit clocking data.

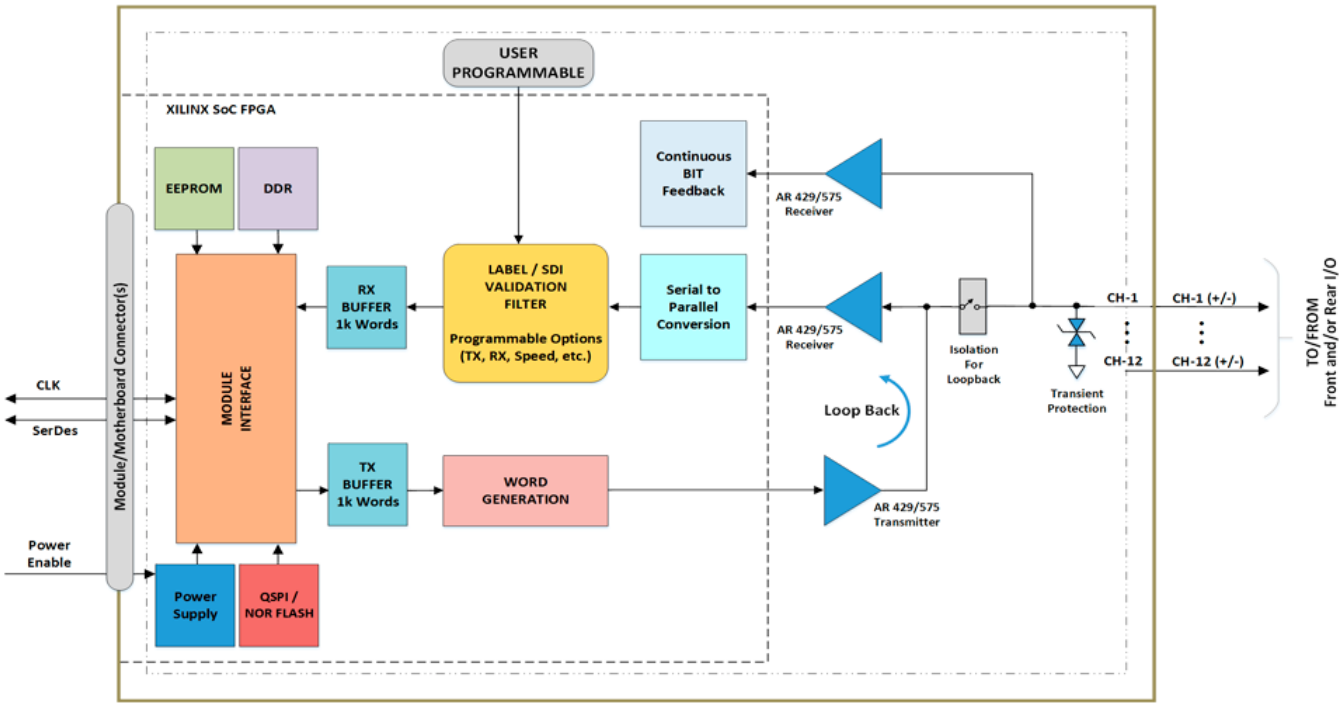
ARINC 575 is a data transfer protocol for the Digital Air Data System (DADS) that provides essential air-data information for displays, autopilots, and other flight controls and instrumentation on commercial and transport type aircraft. ARINC 575 defines a digital data bus to distribute information to displays and other systems. There are minor differences between the digital data bus of ARINC 575 and ARINC 429. The most significant difference is that ARINC 429 reserves bit 32 for parity, while ARINC 575 can use bit 32 for either parity (when BNR) or data (when BCD).

2 Features

- Receive/Transmit mode programmable per channel
- 100 kHz or 12.5 kHz operation per channel
- Transmit: 255 message FIFO or scheduled transmits per channel
- Async transmits during scheduled transmits
- Receive: 255 message FIFO or mailbox buffering per channel
- Message Validation (SDI/Label Filtering) on received messages per channel
- Selectable hardware parity generation/checking
- Receive time stamping
- Continuous BIT
- Loop-back test
- Tri-state outputs
- High and Low speed Slew Rate outputs

3 Specifications

3.1 Module AR1- 12-Channel ARINC 429/575 Communications



Input/Output Format:	Twelve channels, programmed for either Rx or Tx per channel
Frequency:	100 kHz or 12.5 kHz operation (programmable)
Buffers:	Rx/Tx FIFO buffering; SDI/Label Filtering
Self-Test:	Loopback test
Format:	AR429 or 575 programmable/channel
Power:	5 VDC @ 175 mA / ±12 VDC @ 240 mA (estimated typical)
Ground:	Ground return is to system ground
Weight:	1.5 oz. (42 g)

Specifications are subject to change without notice.

Specifications	**ARINC 429**	**ARINC 575**
Mode of Operation	Differential	Differential
Data Rate	100 kHz	12.5 kHz
Driver Output Signal Level (Min Loaded)	±10.0 V	±10.0 V
Receiver Input Voltage Range	-17 V to +17 V	-17 V to +17 V
Receiver Input Resistance (Ohms)	15 K	15 K
Module Supply current, no load (nom):	0.8 A@+5 V; 0.05 A@+12 V; 0.05A@-12 V	
Module Supply current, no load (peak):	1.0 A@+5 V; 0.1 A@+12 V; 0.1A@-12 V	

3.2 Module Factory Defaults

Speed:	12.5 khz
Gap Time:	4 bits
Interrupt Level:	0
Interrupt Vector:	0x00
Transmit Mode:	Immediate FIFO
Receive Mode:	FIFO
Parity (Odd):	Enabled
Receivers:	Disabled
Transmitters:	Disabled
SDI/Label Matching:	Disabled
Number of Words Tx Buffer:	0
Number of Words Rx Buffer:	0
Rx Buffer, Almost Full:	0x80
Tx Buffer, Almost Empty:	0x20
Tx-Rx Configuration High:	0
Tx-Rx Configuration Low:	0
Channel Control High:	0
Channel Control Low:	0
Built-In-Test:	Enabled

4 Principle of Operation

Module AR1 provides up to 12 programmable ARINC-429 channels. Each channel is software selectable for transmit and/or receive, high or low speed, and odd or no parity. Therefore, AR1 can support multiple ARINC 429 and 575 channels simultaneously.

4.1 Receive Operation

Serial BRZ data is decoded for logic states: one, zero or null. Once Word Gap is detected (4 null states) the receiver waits for either a zero or one state to start the serial-to-parallel shift function. If a waveform timing fault is detected before the serial/parallel function is complete, operation is terminated and the receiver returns to waiting for Word Gap detection. The serial-to-parallel output data is validated for odd parity, Label and Serial-to-Digital Interface (SDI).

If message validation (filtering) is enabled, the module compares the SDI/Label of incoming ARINC messages to a list of desired SDI/Labels in validation (match) memory and only stores messages with an SDI/Label in the list. The message is stored in the receive FIFO or mailbox, depending if the channel is in FIFO receive mode or mailbox receive mode. In FIFO Receive Mode, received ARINC messages / words are stored with an associated status word and an optional time-stamp value in the channel's receive FIFO. Additionally, the Rx FIFO can be set for either bounded or circular mode, which determines FIFO behavior when it is full. In bounded mode, newly received ARINC messages are discarded if the FIFO is full whereas in circular mode, new ARINC messages overwrite the oldest messages in the FIFO. In mailbox mode, received ARINC words are stored in mailboxes or records in RAM that are indexed by the SDI/Label of the ARINC word. Each mailbox contains a status word associated with the message, the ARINC message / word, and an optional 32-bit timestamp value. The status word indicates parity error and new message status.

4.2 Transmit Operation

Transmitters are tri-stated when TX is not enabled. Transmit operates in one of three modes: Immediate FIFO, Triggered FIFO, and Scheduled. In immediate mode, ARINC data is sent as soon as data is written to the transmit FIFO. In Triggered FIFO mode, a write to the Transmit Trigger register is needed to start transmission of the transmit FIFO contents. Transmission continues until the FIFO is empty. To transmit more data after the FIFO empties out, issue a new trigger after filling the transmit FIFO with new data.

For either FIFO mode, a transmit FIFO Rate register is provided to control rate of transmission. The contents of this register specify the gap time between transmitted words from the FIFO. The default is the minimum ARINC gap time of 4-bit times.

Schedule mode transmits ARINC data words according to a prebuilt schedule table in Transmit Schedule RAM. In the Schedule table, various commands define what messages are sent and the duration of gaps between each message. Note that a Gap (Gap or Fixed Gap) command must be explicitly added in between each Message command otherwise a gap will not be inserted between messages. The ARINC data words and gap times are stored in the Transmit Message RAM and can be updated on the fly as the schedule executes. A write to the Transmit Trigger register initiates the schedule and commands are executed starting from the first command (address 0x0) in the Schedule RAM. While a schedule is running, an ARINC word can be transmitted asynchronously by writing the async data word to the Async Transmit Data register. After it has transmitted, the Async Data Available bit will be cleared from the Channel Status register and the Async Data Sent Interrupt will be set if enabled. The Async Data Available bit in Channel Status also gets cleared by a Stop Cmd in a schedule or if a Transmit Stop command is issued from the Transmit Stop register. Use the Fixed Gap command instead of the Gap command to disable async transmissions during the schedule gap time. Gap and Fixed Gap commands can both be used when building the transmit schedule.

4.2.1 Schedule Transmit Commands

ARINC 429/575 scheduling is controlled by commands that are written to the Transmit Schedule RAM. The available commands are:

- Message
- Gap
- Fixed Gap
- Pause
- Schedule Interrupt
- Jump
- Stop

1.1.1.1 Message

This command takes a parameter that specifies the location in Transmit Message memory containing the ARINC data word to be sent. The word is transmitted when the Message command is executed. This ARINC word can be modified in Tx Message memory while the schedule is running.

1.1.1.2 Gap

This command takes a parameter that specifies the location in Transmit Message memory containing a 20-bit gap time value. Values less than 4 are invalid. If the previous command was a Message, then that message is transmitted and then the transmitter waits out the specified gap time transmitting nulls. An exception to this is if there is an async data word available. If the gap time is greater or equal to 40 bit times (4-bit gap time plus one ARINC word plus another 4-bit gap time) an async data word, if available, will be transmitted during this time. If a new async data word is made available and the remaining gap time is large enough to accommodate another async data word transmission, then the new async data word will be transmitted after a 4-bit gap time. Multiple async data word transmissions can thus occur as long as the remaining gap time is large enough to accommodate a message and the required minimum 4-bit gap time. Otherwise, the transmitter waits out the remaining gap time before executing the next command.

1.1.1.3 Fixed Gap

This command takes a parameter that specifies the location in Transmit Message memory containing a 20-bit gap time value. Values less than 4 are invalid. If the previous command was a Message, then that message is transmitted with the specified gap time appended. If the previous command was not a Message, then the transmitter waits for the specified gap time before executing the next command. The difference between the Fixed Gap and Gap command is that Fixed Gap will prevent the transmission of async data words during the gap time. Use Fixed Gap to only allow nulls to be transmitted during the gap time.

1.1.1.4 Pause

This command causes the transmitter to pause execution of the schedule after transmitting the current word. Either a Transmit Trigger command is issued to resume execution, or a Transmit Stop command is issued to halt execution.

1.1.1.5 Interrupt

This command causes the Schedule Interrupt to be set if Schedule Interrupt is enabled. An unlatched version of this flag is also visible in the channel status register.

1.1.1.6 Jump

Jumps to the 9-bit address in Schedule memory pointed to by this command and resumes execution there.

1.1.1.7 Stop

This command causes the transmitter to stop execution of the schedule after transmitting the current word.

4.3 ARINC 429/575 Built-in Test

The AR1 module supports three types of built-in tests: Power-On, Continuous Background and Initiated. The results of these tests are logically ORed together and stored in the *BIT Dynamic Status* and *BIT Latched Status* registers.

4.3.1 Power-On Self-Test (POST) / Power-on BIT (PBIT) / Start-up BIT(SBIT)

The power-on self-test is performed on each channel automatically when power is applied and reports the results in the *BIT Status* register when complete. After power-on, the *Power-on BIT Complete* register should be checked to ensure that POST/PBIT/SBIT test is complete before reading the *BIT Dynamic Status* and *BIT Latched Status* registers.

4.3.2 Continuous Background Built-In Test

The background Built-In-Test or Continuous BIT (CBIT) runs in the background for each enabled channel. In Transmit operations, internal transmit data is compared to loop-back data received by the ARINC receivers. When the channel is configured for Receive operation, receive data is continuously monitored via a secondary parallel path circuit and compared to the primary input receive data. If the data does not match, the technique used by the automatic background BIT test consists of an “add-2, subtract-1” counting scheme. The BIT counter is incremented by 2 when a BIT-fault is detected and decremented by 1 when there is no BIT fault detected and the BIT counter is greater than 0. When the BIT counter exceeds the (programmed) *Background BIT Threshold* value, the specific channel’s fault bit in the BIT status register will be set. The “add-2, subtract-1” counting scheme effectively filters momentary or intermittent anomalies by allowing them to “come and go“ before a BIT fault status or indication is flagged (e.g. BIT faults would register when sustained). This prevents spurious faults from registering valid such as those caused by EMI and/or dirty power causing false BIT faults. Putting more “weight” on errors (“add-2”) and less “weight” on subsequent passing results (subtract-1) will result in a BIT failure indication even if a channel “oscillates” between a pass and fail state. Results of the Continuous BIT are stored in the *BIT Dynamic Status* and *BIT Latched Status* register.

4.3.3 Initiated Built-In Test

The Initiated Built-In-Test (IBIT) is an internal loopback available for each channel of the AR1 module. The test is initiated by setting the bit for the associated channel in the *Test Enabled* register to a **1**. Once enabled, they must wait at least 3 msec before checking to see if the bit for the associated channel in the *Test Enabled* register reads a **0**. When the AR1 clears the bit, it means that the test has completed, and its results can be checked. The results of the IBIT is stored in the *BIT Dynamic Status* and *BIT Latched Status* registers, a **0** indicates that the channel has passed and a **1** indicates that it failed.

4.4 Loop-Back Operation

Transmit and receive operation of an AR1 channel can be verified internally by enabling both Tx and Rx on the same channel. Tx Scheduling is not supported when the channel is placed in this mode.

4.5 Transient Protection

The module is normally configured for transient protection but can be specified without if protection is implemented externally.

4.6 Status and Interrupts

The AR1 Module provide registers that indicate faults or events. Refer to “Status and Interrupts Module Manual” for the Principle of Operation description.

5 Register Descriptions

The register descriptions provide the register name, Type, Data Range, Read or Write information, Initialized Value, a description of the function and, in most cases, a data table.

5.1 Receive Registers

The registers listed are associated with data that is received on the AR1 channels. Two modes of message storage are supported: Receive FIFO and Receive Mailbox.

5.1.1 Receive FIFO Mode Registers

The Receive FIFO Mode Registers contain information about ARINC messages that are received via the Receive FIFO buffer on the AR1 channel. The registers associated with this feature are:

- Receive FIFO Message Buffer
- Receive FIFO Message Count
- Receive FIFO Almost Full Threshold
- Receive FIFO Size

5.1.1.1 Receive FIFO Message Buffer

Function: In FIFO receive mode, the received ARINC messages are stored in this buffer.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: R

Initialized Value: NA

Operational Settings: Perform two reads from this register to retrieve the Status word and the ARINC data word, respectively. If Time Stamping is enabled, perform one more read to retrieve the timestamp.

Receive FIFO Message Buffer															
Message Status Word															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**N**	**PE**
Data Word															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**
Timestamp Word (*if enabled)															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

PE = Parity Error '**1**' Calculated parity does not match the received parity bit
N = New message '**1**' Message has not been read yet

5.1.1.2 Receive FIFO Message Count

Function: Contains the number of ARINC messages in the receive FIFO in Receive FIFO mode.

Type: unsigned binary word (32-bit)

Range: 0 to 255

Read/Write: R

Initialized Value: 0

Operational Settings: A received message consists of the message status word and the ARINC data word. If time stamping is enabled, a 32-bit timestamp is also included in the message. For example, if this register reads '1', indicating one message is loaded in the receive FIFO, perform two reads from the Receive FIFO Message Buffer register to retrieve the full message (status word and ARINC data word) if time stamping is disabled or perform three reads from the Receive FIFO Message Buffer register to retrieve the full message (status word, ARINC data word and timestamp word) if time stamping is enabled.

Receive FIFO Message Count															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.1.1.3 Receive FIFO Almost Full Threshold

Function: Specifies the level of the receive FIFO buffer, equal or above, at which the Rx FIFO Almost Full Status bit D1 in the Channel Status register, is flagged (High True).

Type: unsigned binary word (32-bit)

Range: 0 to 255

Read/Write: R/W

Initialized Value: 128 (0x0080)

Operational Settings: If the *Interrupt Enable* register interrupt is enabled, a SYSTEM interrupt will be generated when the receive FIFO level increases and reaches the threshold level. This register does NOT get reset by a channel reset.

Receive FIFO Almost Full Threshold															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.1.1.4 Receive FIFO Size

Function: Specifies the size of the Rx FIFO buffer. The default size is 255 messages.

Type: unsigned binary word (32-bit)

Range: 1 to 255

Read/Write: R/W

Initialized Value: 255 (0xFF)

Operational Settings: This setting affects the Rx FIFO size when the Rx FIFO is configured in either Rx FIFO Bounded or Circular mode.

Receive FIFO Size

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.1.2 Receive Mailbox Mode Registers

The Receive Mailbox Mode Registers contain information about ARINC messages that are received via mailboxes on the AR1 channel. The registers associated with this feature are:

- Receive FIFO SDI/Label Buffer
- Receive FIFO SDI/Label Count
- Receive FIFO Almost Full Threshold
- Receive FIFO Size
- Mailbox Status Data
- Mailbox Message Data
- Mailbox Timestamp Data

5.1.2.1 Receive FIFO SDI/Label Buffer

Function: In Mailbox receive mode, SDI/Label of received messages are stored in this buffer.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 03FF

Read/Write: R

Initialized Value: N/A

Operational Settings: In Mailbox receive mode, this FIFO contains the 10-bit SDI/Label of newly received messages. This provides a list to the user showing which mailboxes contain new messages since the last time this FIFO was read.

Receive FIFO SDI/Label Buffer															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	**A10**	**A9**	**A8**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**

A8-A1 = Label (A8 is MSB and A1 is LSB)
A10-A9 = SDI

5.1.2.2 Receive FIFO SDI/Label Count

Function: Contains the number of newly received SDI/Labels in the receive FIFO in Receive Mailbox mode.

Type: unsigned binary word (32-bit)

Range: 0 to 255

Read/Write: R

Initialized Value: 0

Operational Settings: In Mailbox receive mode, this register contains the number of newly received SDI/Labels in the receive FIFO. The user may perform this number of reads on the Receive FIFO SDI/Label Buffer register to retrieve all SDI/Labels.

Receive FIFO SDI/Label Count															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.1.2.3 Receive FIFO Almost Full Threshold

Function: Specifies the level of the receive FIFO buffer, equal or above, at which the Rx FIFO Almost Full Status bit D1 in the Channel Status register, is flagged (High True).

Type: unsigned binary word (32-bit)

Range: 0 to 255

Read/Write: R/W

Initialized Value: 128 (0x0080)

Operational Settings: If the *Interrupt Enable* register interrupt is enabled, a SYSTEM interrupt will be generated when the receive FIFO level increases and reaches the threshold level. This register does NOT get reset by a channel reset.

Receive FIFO Almost Full Threshold															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.1.2.4 Receive FIFO Size

Function: Specifies the size of the Rx FIFO buffer. The default size is 255 SDI/Labels.

Type: unsigned binary word (32-bit)

Range: 1 to 255

Read/Write: R/W

Initialized Value: 255 (0xFF)

Operational Settings: This setting affects the Rx FIFO size when the Rx FIFO is configured in either Rx FIFO Bounded or Circular mode.

Receive FIFO Size															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.1.2.5 Mailbox Status Data

Function: Stores ARINC Status data word.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 0003

Read/Write: R

Initialized Value: 0

Operational Settings: This is a 32-bit value that contains status information associated with the received ARINC word. D1 of '1' indicates that the received ARINC word is a new message. D0 of '1' indicates a parity error is present in the ARINC message. There are 1024 Mailbox Status Data registers, one for each SDI/Label. The user can determine which Mailbox Status Data registers contain new data based on newly received SDI/Labels in the receive FIFO.

Mailbox Status Data															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**N**	**PE**

PE = Parity Error '**1**' Calculated parity does not match the received parity bit
N = New message '**1**' This is a new ARINC message

5.1.2.6 Mailbox Message Data

Function: Stores ARINC Message data word.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: R

Initialized Value: 0

Operational Settings: This is the 32-bit ARINC data word. There are 1024 Mailbox Message Data registers, one for each SDI/Label. The user can determine which Mailbox Message Data registers contain new data based on newly received SDI/Labels in the receive FIFO.

5.1.2.7 Mailbox Timestamp Data

Function: Stores ARINC Timestamp data word.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: R

Initialized Value: 0

Operational Settings: This is the 32-bit timestamp associated with the received ARINC word. There are 1024 Mailbox Timestamp Data registers, one for each SDI/Label. The user can determine which Mailbox Timestamp Data registers contain new data based on newly received SDI/Labels in the receive FIFO.

5.1.3 Timestamp Registers

1.1.1.8 Timestamp Control

Function: Determines the resolution of the timestamp counter.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 0007

Read/Write: R/W

Initialized Value: 0 (1 µsec)

Operational Settings: The LSB can have one of four time values. Set bit D2 to zero out the timestamp counter.

Timestamp Control															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	D	D	**Z**	**D**	**D**

D1-D0 = Resolution (R/W)
0:0 1 µs
0:1 10 µs
1:0 100 µs
1:1 1 ms
D2 = Zero Timestamp

1.1.1.9 Timestamp Value

Function: Reads the current 32-bit timestamp.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: R

Initialized Value: NA

Operational Settings: The time value of each LSB is determined by the resolution set in the *Timestamp Control* register.

5.1.4 Message Validation Registers

If message validation (filtering) is enabled, the module compares the SDI/Label of incoming ARINC messages to a list of desired SDI/Labels in validation (match) memory and only stores messages with an SDI/Label in the list.

1.1.1.10 Match Enable

Function: Enables or disables reception of ARINC words containing the associated SDI/Label.

Type: unsigned binary word (32-bit)

Range: 0 to 1

Read/Write: R/W

Initialized Value: 0

Operational Settings: D0 set to '1' enables reception of ARINC words containing the SDI/Label that is associated with this register. This register only takes effect if the MATCH ENABLE bit is set to '1' in the Channel Control Register. There are 1024 Match Enable Data Registers and each register is indexed by the SDI/Label. Note that bit D1 is a reserved bit and it is fixed to '1'.

Match Enable															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**D**

5.2 Transmit Registers

The registers listed are associated with data that is to be transmitted from the AR1 channels. Two modes of message storage are supported: Transmit FIFO and Transmit Scheduling.

5.2.1 Transmit FIFO Registers

The Transmit FIFO Mode Registers contain information about ARINC messages that are to be transmitted via the Transmit FIFO buffer on the AR1 channel. The registers associated with this feature are:

- Transmit FIFO Message Buffer
- Transmit FIFO Message Count
- Transmit FIFO Almost Empty Threshold
- Transmit FIFO Rate

5.2.1.1 Transmit FIFO Message Buffer

Function: In immediate or triggered FIFO modes, ARINC messages are placed here prior to transmission.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: W

Initialized Value: N/A

Operational Settings: ARINC data words are 32-bits. This memory is shared with the Tx Message memory and is only available in Tx FIFO modes.

5.2.1.2 Transmit FIFO Message Count

Function: Contains the number of ARINC 32-bit words in the transmit FIFO.

Type: unsigned binary word (32-bit)

Range: 0 to 255

Read/Write: R

Initialized Value: 0

Operational Settings: Used only in the FIFO transmit modes.

Transmit FIFO Message Count															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.2.1.3 Transmit FIFO Almost Empty Threshold

Function: Specifies the level of the transmit buffer, equal or below, at which the Tx FIFO Almost Empty Status bit D5 in the Channel Status register, is flagged (High True).

Type: unsigned binary word (32-bit)

Range: 0 to 255

Read/Write: R/W

Initialized Value: 32 decimal (0x0020)

Operational Settings: If the *Interrupt Enable* register interrupt is enabled, a SYSTEM interrupt will be generated when the receive FIFO level increases and reaches the threshold level. This register does NOT get reset by a channel reset.

Transmit FIFO Almost Empty Threshold

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.2.1.4 Transmit FIFO Rate

Function: Determines the Gap time between transmitted ARINC messages in FIFO transmit modes.

Type: unsigned binary word (32-bit)

Range: 0-0x000F FFFF

Read/Write: R/W

Initialized Value: 4

Mode: FIFO

Operational Settings: Each LSB is 1 bit time. Rates less than 4 are not valid. This register does NOT get reset by a channel reset.

Transmit FIFO Rate															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

5.2.2 Transmit Scheduling Registers

The Transmit Scheduling Registers are utilized when the channel is set up to run a Transmit Schedule. The memories/registers associated with this feature are:

- Transmit Schedule RAM
- Transmit Message RAM
- Async Transmit Data Register

5.2.2.1 Transmit Schedule RAM Command Format

Function: The Transmit Schedule RAM consists of 256 32-bit words that are used to set up a self-running transmit schedule. These are the valid command formats for the Transmit Schedule RAM.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 FFFF

Read/Write: R/W

Initialized Value: N/A

Operational Settings: Only bits 0 to 15 are utilized for schedule commands. Bits 12 to 15 specify the command type and bits 0 to 7 or 8 specify the command parameter. Only the Message, Gap, Fixed Gap and Jump commands utilize a command parameter. When the schedule starts, commands are executed sequentially starting from schedule RAM address 0x0.

Transmit Schedule RAM Command Format																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	STOP CMD
0	**0**	**0**	**1**	0	0	0	**0**	**MA7**	**MA6**	**MA5**	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**	MESSAGE CMD[1]
0	**0**	**1**	**0**	0	0	0	**0**	**MA7**	**MA6**	**MA5**	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**	GAP CMD[1]
0	**0**	**1**	**1**	0	0	0	**0**	**MA7**	**MA6**	**MA5**	**MA4**	**MA3**	**MA2**	**MA1**	**MA0**	FIXED GAP CMD[1]
0	**1**	**0**	**0**	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	PAUSE CMD
0	**1**	**0**	**1**	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	SCH INTERRUPT CMD
0	**1**	**1**	**0**	0	0	0	**SA8**	**SA7**	**SA6**	**SA5**	**SA4**	**SA3**	**SA2**	**SA1**	**SA0**	JUMP CMD[2]
0	**1**	**1**	**1**	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	RESERVED
1	**0**	**0**	**0**	0	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	RESERVED

1. **MA7-MA0** = Address of Tx Message memory organized as 256x32.
2. **SA8-SA0** = Address of next command in Tx Schedule memory organized as 256x32.

5.2.2.2 Transmit Message RAM Data Format

Function: The Transmit Message RAM consists of 256 32-bit words that are used by the transmit schedule for ARINC message and gap time word storage.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: N/A

Operational Settings: Words that are stored in Transmit Message RAM are utilized by Message, Gap and Fixed Gap commands in the Transmit Schedule. In the case of Message commands, the command parameter specifies an address in Transmit Message RAM that contains the 32-bit ARINC message to transmit. In the case of Gap or Fixed Gap commands, the command parameter specifies an address in Transmit Message RAM that contains the gap time value.

5.2.2.3 Async Transmit Data

Function: This memory location is the transmit async buffer.

Type: unsigned binary word (32-bit)

Range: 0 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: While a schedule is running, a single 32-bit ARINC message that is intended to be transmitted asynchronously must be written to this register. When an async data word is written to this register, the Async Data Available status bit will get set until the async data word is transmitted. If a gap (not fixed gap) time is greater or equal to 40 bit times (4-bit gap time plus one ARINC word plus another 4-bit gap time) the async data word, if available, will be transmitted during this time.

5.2.3 Transmit Control Registers

Control of the transmission of ARINC messages includes the ability to start/resume, pause and stop the transmission of the message.

5.2.3.1 *Transmit Trigger*

Function: Sends a trigger command to the transmitter and is used to start transmission in Triggered FIFO or Scheduled Transmit modes.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 0FFF

Read/Write: W

Initialized Value: 0

Operational Settings: Set bit to **1** for the channel to resume transmission after a scheduled pause or Transmit pause command.

Transmit Trigger															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

5.2.3.2 *Transmit Pause*

Function: Sends a command to pause the transmitter after the current word and gap time has finished transmitting.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 0FFF

Read/Write: W

Initialized Value: 0

Modes Affected: Triggered FIFO and Schedule Transmit

Operational Settings: Set bit to **1** for the channel to pause transmission in Triggered FIFO or Scheduled Transmit modes. Issue a Transmit Trigger command to resume transmission or issue a Transmit Stop command to halt transmission.

Transmit Pause															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

5.2.3.3 *Transmit Stop*

Function: Sends a command to stop the transmitter after the current word and gap time has been transmitted.

Type: unsigned binary word (32-bit)

Range: : 0 to 0x0000 0FFF

Read/Write: W

Initialized Value: 0

Modes Affected: All Transmit modes

Operational Settings: Set bit to **1** for the channel to stop transmission.

Transmit Stop															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

5.3 Control Registers

The AR1 control registers provide the ability to reset all the channels in the AR1 module and configuring and controlling individual AR1 channels.

5.3.1 Channel Control

Function: Used to configure and control the channels.

Type: unsigned binary word (32-bit)

Range: See table

Read/Write: R/W

Initialized Value: 0

Operational Settings: When writing to this register, the configuration bits must be maintained when setting the control bits.

Bit(s)	CONTROL FUNCTIONS	Description
D31:D20	RESERVED	Set RESERVED bits to **0**.
D19	CHANNEL RESET	When the CHANNEL RESET bit is set to **1** by the user, the channel is held in reset until the user sets the bit to **0**. The channel reset causes Tx and Rx FIFO buffers to clear out but channel configuration settings remain unchanged.
D18	MATCH MEMORY CLEAR	When the MATCH MEMORY CLEAR bit is set to **1** by the user and if MATCH ENABLE bit is set to **1**, all 1024 SDI/Labels will be disabled in Rx Match Memory, which means all received ARINC messages will be filtered out and discarded. **This is a self-clearing bit. After setting the bit, allow 100 us to complete.**
D17	RECEIVE FIFO CLEAR	When the RECEIVE FIFO CLEAR bit is set to **1** then set to **0** by the user, the Rx FIFO buffer is cleared out and the Rx FIFO count goes to zero.
D16	TRANSMIT FIFO CLEAR	When the TRANSMIT FIFO CLEAR bit is set to **1** then set to **0** by the user, the Tx FIFO buffer is cleared out and the Tx FIFO count goes to zero.

	CONFIGURATION FUNCTIONS	Description/Values
D15:D12	RESERVED	Set RESERVED bits to **0**.
D11	RX FIFO MODE	The Rx FIFO MODE bit can be set to (**1**) in order for the Rx FIFO buffer to operate in circular mode. In this mode, when the FIFO is full, newly received ARINC words will overwrite the oldest data in the FIFO. If the Rx FIFO MODE bit is set to (**0**), the Rx FIFO buffer will operate in bounded mode. In this mode, when the FIFO is full, newly received ARINC words will be discarded. BOUNDED = 0 CIRCULAR = 1
D10	STORE ON ERROR DISABLE	If the STORE ON ERROR DISABLE bit is cleared (**0**) and odd parity is enabled, received words that contain a parity error will be stored in the receive buffer or mailbox. When the STORE ON ERROR DISABLE bit is set (**1**) and odd parity is enabled, received words that contain a

		parity error will NOT be stored in the receive buffer or mailbox.
D9	RESERVED	Set RESERVED bit to **0**.
D8	TIMESTAMP ENABLE	When TIMESTAMP ENABLE bit is set to **1**, the receiver will store a 32-bit time stamp value along with the received ARINC word. There is one time stamp counter per module and it is used across all 12 channels. It has 4 selectable resolutions and can be reset via the *Time Stamp Control* register. It is recommended to clear the Receive FIFOs whenever the Receive mode or Time Stamp Enable mode is changed to ensure that extraneous data is not leftover from a previous receive operation.
D7	MATCH ENABLE	When the MATCH ENABLE bit is set to **1**, the receiver will only store ARINC words which match the SDI/Labels enabled in Rx Match memory.
D6	PARITY DISABLE	The PARITY DISABLE bit when set to **0**, causes ARINC bit 32 to be treated as an odd parity bit. The transmitter calculates the ARINC odd parity bit and transmits it as bit 32. The receiver will check the received ARINC word for odd parity and will flag an error if is not. When the PARITY DISABLE bit is set to **1**, parity generation and checking will be disabled and both the transmitter and receiver will treat ARINC bit 32 as data and pass it on unchanged.
D5	SPEED	The SPEED bit is used to select the data rate. 12.5 kHz = 0 100 kHz = 1
D4:D3	TRANSMIT MODE	The TRANSMIT MODE bits are used to select the Transmit Mode. (0:0) = Immediate FIFO mode (0:1) = Schedule mode (1:0) = Triggered FIFO mode (1:1) = Invalid mode
D2	TRANSMIT ENABLE	The TRANSMIT ENABLE bit should be set after all transmit parameters have been set up. This is especially important in Immediate FIFO Transmit mode, since this mode will start transmitting as soon as data is put into the Tx FIFO.
D1	RECEIVE MODE	The RECEIVE MODE bit is used to select the storage mode (FIFO or Mailbox) of received messages. FIFO = 0 MBOX = 1
D0	RECEIVER ENABLE	The RECEIVER ENABLE bit should be set after all receive parameters and filters have been set up. After setting this bit, the module will look for a minimum 4-bit gap time before decoding any ARINC bits to prevent it from receiving a partial ARINC word.

5.3.2 Module Reset

Function: Sends a command to reset the entire 12-channel module to power up conditions.

Type: unsigned binary word (32-bit)

Range: 0 or 1

Read/Write: W

Initialized Value: 0

Operational Settings: All FIFOs are cleared. However, it does not clear out any memories. Set D0 to **1** to reset the module then set to **0** to bring it out of reset.

Module Reset															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**

5.4 ARINC 429/575 Test Registers

The AR1 module provides the ability to run an initiated test (IBIT). Writing a **1** to the bit associated with the channel in the *Test Enabled* register.

5.4.1 Test Enabled

Function: Set the bit corresponding to the channel you want to run Initiated Built-In-Test.

Type: unsigned binary word (32-bit)

Data Range: 0 to 0x0000 0FFF

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: Set bit to **1** for channel to run an Initiated BIT test. Failures in the BIT test are reflected in the *BIT Status* registers for the corresponding channels that fail. In addition, an interrupt (if enabled in the *BIT Interrupt Enable* register) can be triggered when the BIT testing detects failures. Bit is self-clearing and does so upon completion of the test. Allow at least 3 ms per channel for the test enabled bits to clear after enabling. Note that running Initiated BIT test on a channel will interrupt operation of the channel and all FIFOs will get cleared. The system implementation should take this behavior into consideration.

Test Enabled															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

5.5 Background BIT Threshold Programming Registers

The *Background BIT Threshold* register provides the ability to specify the ***minimum*** time before the BIT fault is reported in the *BIT Status* registers. The *Reset BIT* register provides the ability to reset the BIT counter used in CBIT.

5.5.1 Background BIT Threshold

Function: Sets background BIT Threshold value to use for all channels for BIT failure indication.

Data Range: 1 to 65,535

Read/Write: R/W

Initialized Value: 5

Operational Settings: This value represents the background BIT error “count” that, when surpassed, will cause the BIT status to indicate failure.

5.5.2 Reset BIT

Function: Resets the CBIT internal circuitry and count mechanism. Set the bit corresponding to the channel you want to clear.

Type: unsigned binary word (32-bit)

Data Range: 0 to 0x0000 0FFF
Read/Write: W
Initialized Value: 0
Operational Settings: Set bit to **1** for channel to resets the CBIT mechanisms. Bit is self-clearing.

Reset BIT															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

5.6 Status and Interrupt Registers

The AR1 Module provides status registers for BIT and Channel.

5.6.1 BIT Status

There are four registers associated with the BIT Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt.*

BIT Dynamic Status															
BIT Latched Status															
BIT Interrupt Enable															
BIT Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

Function: Sets the corresponding bit associated with the channel's BIT register.
Type: unsigned binary word (32-bit)
Data Range: 0x0000 0000 to 0x0000 0FFF
Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)
Initialized Value: 0

5.6.2 Channel Status

There are four registers associated with the Channel Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt.* Use this register to read current or real-time status. The Built-In-Test Error bit is latched and will stay set once an error is detected. It can be cleared by reading the BIT Status register. The Schedule Interrupt bit can be cleared by reading the Interrupt Status register when enabled or it can be cleared via the *Channel Control* register. See specific registers for function description and programming.

The Rx Data Available bit is set when the receive FIFO is not empty. The Rx FIFO Overflow bit will set whenever the receiver has to discard data because the receive FIFO was full and new data was received. The Async Data Available bit in Channel Status also gets cleared by a Stop Cmd in a schedule or if a Transmit Stop command is issued from the Transmit Stop register. The Tx Run bit is set whenever the transmitter is executing a schedule or actively transmitting the contents of the transmit FIFO. The Tx Pause bit is set whenever the transmitter has been paused in schedule mode. Some events are NOT latched. They are dynamic.

Bit	Description	Configurable?	Configuration Register
D0	Rx Data Available	No	
D1	Rx FIFO Almost Full	Yes	Receive FIFO Almost Full Threshold
D2	Rx FIFO Full	Yes	Receive FIFO Size
D3	Rx FIFO Overflow	Yes	Receive FIFO Size
D4	Tx FIFO Empty	No	
D5	Tx FIFO Almost Empty	Yes	Transmit FIFO Almost Empty Threshold
D6	Tx FIFO Full	No	
D7	Parity Error	No	
D8	Receive Error	No	
D9	Built-in-Test Error	No	
D10	Schedule Interrupt	No	
D11	Async Data Available	No	
D12	Tx Run	No	
D13	Tx Pause	No	

Channel Dynamic Status															
Channel Latched Status															
Channel Interrupt Enable															
Channel Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**

Function: Sets the corresponding bit associated with the event type. There are separate registers for each channel.

Type: unsigned binary word (32-bit)

Range: 0 to 0x0000 3FFF

Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)

Initialized Value: N/A

5.6.3 Summary Status

Function: Sets the corresponding bit associated with the channel that has data available to receive in its *Receive FIFO Mode* or *Receive Mailbox Mode* registers.

Type: unsigned binary word (32-bits)

Data Range: 0x0000 0000 to 0x0000 0FFF

Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Set Edge/Level Interrupt*)

Initialized Value: 0

Summary Dynamic Status															
Summary Latched Status															
Summary Interrupt Enable															
Summary Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	**Ch12**	**Ch11**	**Ch10**	**Ch9**	**Ch8**	**Ch7**	**Ch6**	**Ch5**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

Summary Events Table

Module	BIT	Overcurrent	External Power Loss	Open Line	External Power Under Volt	External Power Over Volt	Over Temp	Surge Suppressor Fault	Receive Data Available
AR1									X

5.6.4 Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed (typically with a unique number/identifier) such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism.

In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

Note, the Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Common Memory and these registers are associated with the Module Slot position (refer to Function Register Map).

5.6.4.1 Interrupt Vector

Function: Set an identifier for the interrupt.

Type: unsigned binary word (32-bit)

Data Range: 0 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When an interrupt occurs, this value is reported as part of the interrupt mechanism.

5.6.4.2 Interrupt Steering

Function: Sets where to direct the interrupt.

Type: unsigned binary word (32-bit)

Data Range: See table

Read/Write: R/W

Initialized Value: 0

Operational Settings: When an interrupt occurs, the interrupt is sent as specified:

Direct Interrupt to VME	1
Direct Interrupt to ARM Processor (via SerDes) *(Custom App on ARM or NAI Ethernet Listener App)*	2
Direct Interrupt to PCIe Bus	5
Direct Interrupt to cPCI Bus	6

6 Function Register Map

Key: *Regular Italic = Incoming Data*

Regular Underline = Outgoing Data

Bold Italic = Configuration/Control

Bold Underline = Status

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e., write-1-to-clear, writing a "1" to a bit set to "1" will set the bit to "0).

6.1 Receive Registers

6.1.1 Receive FIFO Mode Registers

0x1104	*Receive FIFO Message Buffer Ch 1*	R
0x1204	*Receive FIFO Message Buffer Ch 2*	R
0x1304	*Receive FIFO Message Buffer Ch 3*	R
0x1404	*Receive FIFO Message Buffer Ch 4*	R
0x1504	*Receive FIFO Message Buffer Ch 5*	R
0x1604	*Receive FIFO Message Buffer Ch 6*	R
0x1704	*Receive FIFO Message Buffer Ch 7*	R
0x1804	*Receive FIFO Message Buffer Ch 8*	R
0x1904	*Receive FIFO Message Buffer Ch 9*	R
0x1A04	*Receive FIFO Message Buffer Ch 10*	R
0x1B04	*Receive FIFO Message Buffer Ch 11*	R
0x1C04	*Receive FIFO Message Buffer Ch 12*	R

0x1110	**Receive FIFO Message Count Ch 1**	R
0x1210	**Receive FIFO Message Count Ch 2**	R
0x1310	**Receive FIFO Message Count Ch 3**	R
0x1410	**Receive FIFO Message Count Ch 4**	R
0x1510	**Receive FIFO Message Count Ch 5**	R
0x1610	**Receive FIFO Message Count Ch 6**	R
0x1710	**Receive FIFO Message Count Ch 7**	R
0x1810	**Receive FIFO Message Count Ch 8**	R
0x1910	**Receive FIFO Message Count Ch 9**	R
0x1A10	**Receive FIFO Message Count Ch 10**	R
0x1B10	**Receive FIFO Message Count Ch 11**	R
0x1C10	**Receive FIFO Message Count Ch 12**	R

0x1108	***Receive FIFO Almost Full Threshold Ch 1***	R/W
0x1208	***Receive FIFO Almost Full Threshold Ch 2***	R/W
0x1308	***Receive FIFO Almost Full Threshold Ch 3***	R/W
0x1408	***Receive FIFO Almost Full Threshold Ch 4***	R/W
0x1508	***Receive FIFO Almost Full Threshold Ch 5***	R/W
0x1608	***Receive FIFO Almost Full Threshold Ch 6***	R/W
0x1708	***Receive FIFO Almost Full Threshold Ch 7***	R/W
0x1808	***Receive FIFO Almost Full Threshold Ch 8***	R/W
0x1908	***Receive FIFO Almost Full Threshold Ch 9***	R/W
0x1A08	***Receive FIFO Almost Full Threshold Ch 10***	R/W
0x1B08	***Receive FIFO Almost Full Threshold Ch 11***	R/W
0x1C08	***Receive FIFO Almost Full Threshold Ch 12***	R/W

0x1124	***Receive FIFO Size Ch 1***	R/W
0x1224	***Receive FIFO Size Ch 2***	R/W
0x1324	***Receive FIFO Size Ch 3***	R/W
0x1424	***Receive FIFO Size Ch 4***	R/W
0x1524	***Receive FIFO Size Ch 5***	R/W
0x1624	***Receive FIFO Size Ch 6***	R/W
0x1724	***Receive FIFO Size Ch 7***	R/W
0x1824	***Receive FIFO Size Ch 8***	R/W
0x1924	***Receive FIFO Size Ch 9***	R/W
0x1A24	***Receive FIFO Size Ch 10***	R/W
0x1B24	***Receive FIFO Size Ch 11***	R/W
0x1C24	***Receive FIFO Size Ch 12***	R/W

6.1.2 Receive Mailbox Mode Registers

0x1104	*Receive FIFO SDI/Label Buffer Ch 1*	R
0x1204	*Receive FIFO SDI/Label Buffer Ch 2*	R
0x1304	*Receive FIFO SDI/Label Buffer Ch 3*	R
0x1404	*Receive FIFO SDI/Label Buffer Ch 4*	R
0x1504	*Receive FIFO SDI/Label Buffer Ch 5*	R
0x1604	*Receive FIFO SDI/Label Buffer Ch 6*	R
0x1704	*Receive FIFO SDI/Label Buffer Ch 7*	R
0x1804	*Receive FIFO SDI/Label Buffer Ch 8*	R
0x1904	*Receive FIFO SDI/Label Buffer Ch 9*	R
0x1A04	*Receive FIFO SDI/Label Buffer Ch 10*	R
0x1B04	*Receive FIFO SDI/Label Buffer Ch 11*	R
0x1C04	*Receive FIFO SDI/Label Buffer Ch 12*	R

0x1110	**Receive FIFO SDI/Label Count Ch 1**	R
0x1210	**Receive FIFO SDI/Label Count Ch 2**	R
0x1310	**Receive FIFO SDI/Label Count Ch 3**	R
0x1410	**Receive FIFO SDI/Label Count Ch 4**	R
0x1510	**Receive FIFO SDI/Label Count Ch 5**	R
0x1610	**Receive FIFO SDI/Label Count Ch 6**	R
0x1710	**Receive FIFO SDI/Label Count Ch 7**	R
0x1810	**Receive FIFO SDI/Label Count Ch 8**	R
0x1910	**Receive FIFO SDI/Label Count Ch 9**	R
0x1A10	**Receive FIFO SDI/Label Count Ch 10**	R
0x1B10	**Receive FIFO SDI/Label Count Ch 11**	R
0x1C10	**Receive FIFO SDI/Label Count Ch 12**	R

0x1108	***Receive FIFO Almost Full Threshold Ch 1***	R/W
0x1208	***Receive FIFO Almost Full Threshold Ch 2***	R/W
0x1308	***Receive FIFO Almost Full Threshold Ch 3***	R/W
0x1408	***Receive FIFO Almost Full Threshold Ch 4***	R/W
0x1508	***Receive FIFO Almost Full Threshold Ch 5***	R/W
0x1608	***Receive FIFO Almost Full Threshold Ch 6***	R/W
0x1708	***Receive FIFO Almost Full Threshold Ch 7***	R/W
0x1808	***Receive FIFO Almost Full Threshold Ch 8***	R/W
0x1908	***Receive FIFO Almost Full Threshold Ch 9***	R/W
0x1A08	***Receive FIFO Almost Full Threshold Ch 10***	R/W
0x1B08	***Receive FIFO Almost Full Threshold Ch 11***	R/W
0x1C08	***Receive FIFO Almost Full Threshold Ch 12***	R/W

0x1124	***Receive FIFO Size Ch 1***	R/W
0x1224	***Receive FIFO Size Ch 2***	R/W
0x1324	***Receive FIFO Size Ch 3***	R/W
0x1424	***Receive FIFO Size Ch 4***	R/W
0x1524	***Receive FIFO Size Ch 5***	R/W
0x1624	***Receive FIFO Size Ch 6***	R/W
0x1724	***Receive FIFO Size Ch 7***	R/W
0x1824	***Receive FIFO Size Ch 8***	R/W
0x1924	***Receive FIFO Size Ch 9***	R/W
0x1A24	***Receive FIFO Size Ch 10***	R/W
0x1B24	***Receive FIFO Size Ch 11***	R/W
0x1C24	***Receive FIFO Size Ch 12***	R/W

0x40000	Mailbox Ch 1	R
0x44000	Mailbox Ch 2	R
0x48000	Mailbox Ch 3	R
0x4C000	Mailbox Ch 4	R
0x50000	Mailbox Ch 5	R
0x54000	Mailbox Ch 6	R
0x58000	Mailbox Ch 7	R
0x5C000	Mailbox Ch 8	R
0x60000	Mailbox Ch 9	R
0x64000	Mailbox Ch 10	R
0x68000	Mailbox Ch 11	R
0x6C000	Mailbox Ch 12	R

0x0000	SDI/Label 0	R
0x0010	SDI/Label 1	R
0x0020	SDI/Label 2	R
…	SD1/Label N	R
0x3FD0	SD1/Label 1021	R
0x3FE0	SD1/Label 1022	R
0x3FF0	SD1/Label 1023	R

0x0000	*Mailbox Status Data*	R
0x0004	*Mailbox Message Data*	R
0x0008	*Mailbox Timestamp Data*	R

6.1.3 Timestamp Registers

0x100C	***Timestamp Control***	R/W
0x1010	**Timestamp Value**	R

6.1.4 Message Validation Registers

0x40000	Validation Memory Ch 1	R
0x44000	Validation Memory Ch 2	R
0x48000	Validation Memory Ch 3	R
0x4C000	Validation Memory Ch 4	R
0x50000	Validation Memory Ch 5	R
0x54000	Validation Memory Ch 6	R
0x58000	Validation Memory Ch 7	R
0x5C000	Validation Memory Ch 8	R
0x60000	Validation Memory Ch 9	R
0x64000	Validation Memory Ch 10	R
0x68000	Validation Memory Ch 11	R
0x6C000	Validation Memory Ch 12	R

0x0000	SDI/Label 0	R
0x0010	SDI/Label 1	R
0x0020	SDI/Label 2	R
…	SD1/Label N	R
0x3FD0	SD1/Label 1021	R
0x3FE0	SD1/Label 1022	R
0x3FF0	SD1/Label 1023	R

0x000C	***Match Enable***	W

6.2 Transmit Registers

6.2.1 Transmit FIFO Registers

0x1100	Transmit FIFO Message Buffer Ch 1	W
0x1200	Transmit FIFO Message Buffer Ch 2	W
0x1300	Transmit FIFO Message Buffer Ch 3	W
0x1400	Transmit FIFO Message Buffer Ch 4	W
0x1500	Transmit FIFO Message Buffer Ch 5	W
0x1600	Transmit FIFO Message Buffer Ch 6	W
0x1700	Transmit FIFO Message Buffer Ch 7	W
0x1800	Transmit FIFO Message Buffer Ch 8	W
0x1900	Transmit FIFO Message Buffer Ch 9	W
0x1A00	Transmit FIFO Message Buffer Ch 10	W
0x1B00	Transmit FIFO Message Buffer Ch 11	W
0x1C00	Transmit FIFO Message Buffer Ch 12	W

0x1114	**Transmit FIFO Message Count Ch 1**	R
0x1214	**Transmit FIFO Message Count Ch 2**	R
0x1314	**Transmit FIFO Message Count Ch 3**	R
0x1414	**Transmit FIFO Message Count Ch 4**	R
0x1514	**Transmit FIFO Message Count Ch 5**	R
0x1614	**Transmit FIFO Message Count Ch 6**	R
0x1714	**Transmit FIFO Message Count Ch 7**	R
0x1814	**Transmit FIFO Message Count Ch 8**	R
0x1914	**Transmit FIFO Message Count Ch 9**	R
0x1A14	**Transmit FIFO Message Count Ch 10**	R
0x1B14	**Transmit FIFO Message Count Ch 11**	R
0x1C14	**Transmit FIFO Message Count Ch 12**	R

0x110C	***Transmit FIFO Almost Empty Threshold Ch 1***	R/W
0x120C	***Transmit FIFO Almost Empty Threshold Ch 2***	R/W
0x130C	***Transmit FIFO Almost Empty Threshold Ch 3***	R/W
0x140C	***Transmit FIFO Almost Empty Threshold Ch 4***	R/W
0x150C	***Transmit FIFO Almost Empty Threshold Ch 5***	R/W
0x160C	***Transmit FIFO Almost Empty Threshold Ch 6***	R/W
0x170C	***Transmit FIFO Almost Empty Threshold Ch 7***	R/W
0x180C	***Transmit FIFO Almost Empty Threshold Ch 8***	R/W
0x190C	***Transmit FIFO Almost Empty Threshold Ch 9***	R/W
0x1A0C	***Transmit FIFO Almost Empty Threshold Ch 10***	R/W
0x1B0C	***Transmit FIFO Almost Empty Threshold Ch 11***	R/W
0x1C0C	***Transmit FIFO Almost Empty Threshold Ch 12***	R/W

0x111C	***Transmit FIFO Rate Ch 1***	R/W
0x121C	***Transmit FIFO Rate Ch 2***	R/W
0x131C	***Transmit FIFO Rate Ch 3***	R/W
0x141C	***Transmit FIFO Rate Ch 4***	R/W
0x151C	***Transmit FIFO Rate Ch 5***	R/W
0x161C	***Transmit FIFO Rate Ch 6***	R/W
0x171C	***Transmit FIFO Rate Ch 7***	R/W
0x181C	***Transmit FIFO Rate Ch 8***	R/W
0x191C	***Transmit FIFO Rate Ch 9***	R/W
0x1A1C	***Transmit FIFO Rate Ch 10***	R/W
0x1B1C	***Transmit FIFO Rate Ch 11***	R/W
0x1C1C	***Transmit FIFO Rate Ch 12***	R/W

6.2.2 Transmit Scheduling Registers

0x80000	Transmit Scheduling Ch 1	R/W
0x81000	Transmit Scheduling Ch 2	R/W
0x82000	Transmit Scheduling Ch 3	R/W
0x83000	Transmit Scheduling Ch 4	R/W
0x84000	Transmit Scheduling Ch 5	R/W
0x85000	Transmit Scheduling Ch 6	R/W
0x86000	Transmit Scheduling Ch 7	R/W
0x87000	Transmit Scheduling Ch 8	R/W
0x88000	Transmit Scheduling Ch 9	R/W
0x89000	Transmit Scheduling Ch 10	R/W
0x8A000	Transmit Scheduling Ch 11	R/W
0x8B000	Transmit Scheduling Ch 12	R/W

0x0000	***Transmit Schedule Command 0***	R/W
0x0004	***Transmit Schedule Command 1***	R/W
…	***Transmit Schedule Command N***	R/W
0x07F8	***Transmit Schedule Command 510***	R/W
0x07FC	***Transmit Schedule Command 511***	R/W

0x90000	Transmit Message RAM Ch 1	R/W

0x0000	***Transmit Message Data Address 0***	R/W

0x91000	Transmit Message RAM Ch 2	R/W
0x92000	Transmit Message RAM Ch 3	R/W
0x93000	Transmit Message RAM Ch 4	R/W
0x94000	Transmit Message RAM Ch 5	R/W
0x95000	Transmit Message RAM Ch 6	R/W
0x96000	Transmit Message RAM Ch 7	R/W
0x97000	Transmit Message RAM Ch 8	R/W
0x98000	Transmit Message RAM Ch 9	R/W
0x99000	Transmit Message RAM Ch 10	R/W
0x9A000	Transmit Message RAM Ch 11	R/W
0x9B000	Transmit Message RAM Ch 12	R/W

0x0004	***Transmit Message Data Address 1***	R/W
…	***Transmit Message Data Address N***	R/W
0x03F8	***Transmit Message Data Address 254***	R/W
0x03FC	***Transmit Message Data Address 255***	R/W

0x1120	Async Transmit Data Ch 1	R/W
0x1220	Async Transmit Data Ch 2	R/W
0x1320	Async Transmit Data Ch 3	R/W
0x1420	Async Transmit Data Ch 4	R/W
0x1520	Async Transmit Data Ch 5	R/W
0x1620	Async Transmit Data Ch 6	R/W
0x1720	Async Transmit Data Ch 7	R/W
0x1820	Async Transmit Data Ch 8	R/W
0x1920	Async Transmit Data Ch 9	R/W
0x1A20	Async Transmit Data Ch 10	R/W
0x1B20	Async Transmit Data Ch 11	R/W
0x1C20	Async Transmit Data Ch 12	R/W

6.2.3 Transmit Control Registers

All Channels		
0x1000	***Tx Trigger***	W
0x1004	***Tx Pause***	W
0x1008	***Tx Stop***	W

6.3 Control Registers

0x1118	*Channel Control Ch 1*	R/W
0x1218	*Channel Control Ch 2*	R/W
0x1318	*Channel Control Ch 3*	R/W
0x1418	*Channel Control Ch 4*	R/W
0x1518	*Channel Control Ch 5*	R/W
0x1618	*Channel Control Ch 6*	R/W
0x1718	*Channel Control Ch 7*	R/W
0x1818	*Channel Control Ch 8*	R/W
0x1918	*Channel Control Ch 9*	R/W
0x1A18	*Channel Control Ch 10*	R/W
0x1B18	*Channel Control Ch 11*	R/W
0x1C18	*Channel Control Ch 12*	R/W

All Channels		
0x1014	*Module Reset*	W

6.4 BIT

0x0800	Dynamic Status	R
0x0804	Latched Status*	R/W
0x0808	*Interrupt Enable*	R/W
0x080C	*Set Edge/Level Interrupt*	R/W

0x0248	*Test Enabled*	R/W

0x02B8	*Background BIT Threshold*	R/W
0x02BC	*Reset BIT*	W

0x02AC	Power-on BIT Complete++	R

++After power-on, Power-on BIT Complete should be checked before reading the BIT Latched Status.

6.5 Channel Status

Ch 1	0x0810	Dynamic Status	R	**Ch 7**	0x0870	Dynamic Status	R
	0x0814	Latched Status*	R/W		0x0874	Latched Status*	R/W
	0x0818	*Interrupt Enable*	R/W		0x0878	*Interrupt Enable*	R/W
	0x081C	*Set Edge/Level Interrupt*	R/W		0x087C	*Set Edge/Level Interrupt*	R/W
Ch 2	0x0820	Dynamic Status	R	**Ch 8**	0x0880	Dynamic Status	R
	0x0824	Latched Status*	R/W		0x0884	Latched Status*	R/W
	0x0828	*Interrupt Enable*	R/W		0x0888	*Interrupt Enable*	R/W
	0x082C	*Set Edge/Level Interrupt*	R/W		0x088C	*Set Edge/Level Interrupt*	R/W
Ch 3	0x0830	Dynamic Status	R	**Ch 9**	0x0890	Dynamic Status	R
	0x0834	Latched Status*	R/W		0x0894	Latched Status*	R/W
	0x0838	*Interrupt Enable*	R/W		0x0898	*Interrupt Enable*	R/W
	0x083C	*Set Edge/Level Interrupt*	R/W		0x089C	*Set Edge/Level Interrupt*	R/W
Ch 4	0x0840	Dynamic Status	R	**Ch 10**	0x08A0	Dynamic Status	R

	0x0844	**Latched Status***	R/W		0x08A4	**Latched Status***	R/W
	0x0848	***Interrupt Enable***	R/W		0x08A8	***Interrupt Enable***	R/W
	0x084C	***Set Edge/Level Interrupt***	R/W		0x08AC	***Set Edge/Level Interrupt***	R/W
Ch 5	0x0850	**Dynamic Status**	R	**Ch 11**	0x08B0	**Dynamic Status**	R
	0x0854	**Latched Status***	R/W		0x08B4	**Latched Status***	R/W
	0x0858	***Interrupt Enable***	R/W		0x08B8	***Interrupt Enable***	R/W
	0x085C	***Set Edge/Level Interrupt***	R/W		0x08BC	***Set Edge/Level Interrupt***	R/W
Ch 6	0x0860	**Dynamic Status**	R	**Ch 12**	0x08C0	**Dynamic Status**	R
	0x0864	**Latched Status***	R/W		0x08C4	**Latched Status***	R/W
	0x0868	***Interrupt Enable***	R/W		0x08C8	***Interrupt Enable***	R/W
	0x086C	***Set Edge/Level Interrupt***	R/W		0x08CC	***Set Edge/Level Interrupt***	R/W

6.6 Interrupt Registers

The Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Memory Space and these addresses are absolute based on the module slot position. In other words, do not apply the Module Address offset to these addresses.

0x0500	***Module 1 Interrupt Vector 1 - BIT***	R/W
0x0504	***Module 1 Interrupt Vector 2 - Channel Status Ch 1***	R/W
0x0508	***Module 1 Interrupt Vector 3 – Channel Status Ch 2***	R/W
0x050C	***Module 1 Interrupt Vector 4 – Channel Status Ch 3***	R/W
0x0510	***Module 1 Interrupt Vector 5 – Channel Status Ch 4***	R/W
0x0514	***Module 1 Interrupt Vector 6 – Channel Status Ch 5***	R/W
0x0518	***Module 1 Interrupt Vector 7 – Channel Status Ch 6***	R/W
0x051C	***Module 1 Interrupt Vector 8 – Channel Status Ch 7***	R/W
0x0520	***Module 1 Interrupt Vector 9 – Channel Status Ch 8***	R/W
0x0524	***Module 1 Interrupt Vector 10 – Channel Status Ch 9***	R/W
0x0528	***Module 1 Interrupt Vector 11 – Channel Status Ch 10***	R/W
0x052C	***Module 1 Interrupt Vector 12 – Channel Status Ch 11***	R/W
0x0530	***Module 1 Interrupt Vector 13 – Channel Status Ch 12***	R/W
0x0534 to 0x0564	***Module 1 Interrupt Vector 14 to 26 - Reserved***	R/W
0x0568	***Module 1 Interrupt Vector 27 – Summary Status***	R/W
0x056C to 0x057C	***Module 1 Interrupt Vector 28 to 32 - Reserved***	R/W

0x0600	***Module 1 Interrupt Steering 1 - BIT***	R/W
0x0604	***Module 1 Interrupt Steering 2 - Channel Status Ch 1***	R/W
0x0608	***Module 1 Interrupt Steering 3 - Channel Status Ch 2***	R/W
0x060C	***Module 1 Interrupt Steering 4 - Channel Status Ch 3***	R/W
0x0610	***Module 1 Interrupt Steering 5 - Channel Status Ch 4***	R/W
0x0614	***Module 1 Interrupt Steering 6 - Channel Status Ch 5***	R/W
0x0618	***Module 1 Interrupt Steering 7 - Channel Status Ch 6***	R/W
0x061C	***Module 1 Interrupt Steering 8 - Channel Status Ch 7***	R/W
0x0620	***Module 1 Interrupt Steering 9 - Channel Status Ch 8***	R/W
0x0624	***Module 1 Interrupt Steering 10 - Channel Status Ch 9***	R/W
0x0628	***Module 1 Interrupt Steering 11 - Channel Status Ch 10***	R/W
0x062C	***Module 1 Interrupt Steering 12 - Channel Status Ch 11***	R/W
0x0630	***Module 1 Interrupt Steering 13 - Channel Status Ch 12***	R/W
0x0634 to 0x0664	***Module 1 Interrupt Steering 14 to 26 - Reserved***	R/W
0x0668	***Module 1 Interrupt Steering 27 – Summary Status***	R/W
0x066C to 0x067C	***Module 1 Interrupt Steering 28 to 32 – Reserved***	R/W

0x0700	***Module 2 Interrupt Vector 1 - BIT***	R/W
0x0704	***Module 2 Interrupt Vector 2 - Channel Status Ch 1***	R/W
0x0708	***Module 2 Interrupt Vector 3 – Channel Status Ch 2***	R/W
0x070C	***Module 2 Interrupt Vector 4 – Channel Status Ch 3***	R/W
0x0710	***Module 2 Interrupt Vector 5 – Channel Status Ch 4***	R/W
0x0714	***Module 2 Interrupt Vector 6 – Channel Status Ch 5***	R/W
0x0718	***Module 2 Interrupt Vector 7 – Channel Status Ch 6***	R/W
0x071C	***Module 2 Interrupt Vector 8 – Channel Status Ch 7***	R/W
0x0720	***Module 2 Interrupt Vector 9 – Channel Status Ch 8***	R/W
0x0724	***Module 2 Interrupt Vector 10 – Channel Status Ch 9***	R/W

0x0800	***Module 2 Interrupt Steering 1 - BIT***	R/W
0x0804	***Module 2 Interrupt Steering 2 - Channel Status Ch 1***	R/W
0x0808	***Module 2 Interrupt Steering 3 - Channel Status Ch 2***	R/W
0x080C	***Module 2 Interrupt Steering 4 - Channel Status Ch 3***	R/W
0x0810	***Module 2 Interrupt Steering 5 - Channel Status Ch 4***	R/W
0x0814	***Module 2 Interrupt Steering 6 - Channel Status Ch 5***	R/W
0x0818	***Module 2 Interrupt Steering 7 - Channel Status Ch 6***	R/W
0x081C	***Module 2 Interrupt Steering 8 - Channel Status Ch 7***	R/W
0x0820	***Module 2 Interrupt Steering 9 - Channel Status Ch 8***	R/W
0x0824	***Module 2 Interrupt Steering 10 - Channel Status Ch 9***	R/W

0x0728	*Module 2 Interrupt Vector 11 – Channel Status Ch 10*	R/W
0x072C	*Module 2 Interrupt Vector 12 – Channel Status Ch 11*	R/W
0x0730	*Module 2 Interrupt Vector 13 – Channel Status Ch 12*	R/W
0x0734 to 0x0764	*Module 2 Interrupt Vector 14 to 26 - Reserved*	R/W
0x0768	*Module 2 Interrupt Vector 27 – Summary Status*	R/W
0x076C to 0x077C	*Module 2 Interrupt Vector 28 to 32 - Reserved*	R/W

0x0828	*Module 2 Interrupt Steering 11 - Channel Status Ch 10*	R/W
0x082C	*Module 2 Interrupt Steering 12 - Channel Status Ch 11*	R/W
0x0830	*Module 2 Interrupt Steering 13 - Channel Status Ch 12*	R/W
0x0834 to 0x0864	*Module 2 Interrupt Steering 14 to 26 - Reserved*	R/W
0x0868	*Module 2 Interrupt Steering 27 – Summary Status*	R/W
0x086C to 0x087C	*Module 2 Interrupt Steering 28 to 32 – Reserved*	R/W

0x0900	*Module 3 Interrupt Vector 1 - BIT*	R/W
0x0904	*Module 3 Interrupt Vector 2 - Channel Status Ch 1*	R/W
0x0908	*Module 3 Interrupt Vector 3 – Channel Status Ch 2*	R/W
0x090C	*Module 3 Interrupt Vector 4 – Channel Status Ch 3*	R/W
0x0910	*Module 3 Interrupt Vector 5 – Channel Status Ch 4*	R/W
0x0914	*Module 3 Interrupt Vector 6 – Channel Status Ch 5*	R/W
0x0918	*Module 3 Interrupt Vector 7 – Channel Status Ch 6*	R/W
0x091C	*Module 3 Interrupt Vector 8 – Channel Status Ch 7*	R/W
0x0920	*Module 3 Interrupt Vector 9 – Channel Status Ch 8*	R/W
0x0924	*Module 3 Interrupt Vector 10 – Channel Status Ch 9*	R/W
0x0928	*Module 3 Interrupt Vector 11 – Channel Status Ch 10*	R/W
0x092C	*Module 3 Interrupt Vector 12 – Channel Status Ch 11*	R/W
0x0930	*Module 3 Interrupt Vector 13 – Channel Status Ch 12*	R/W
0x0934 to 0x0964	*Module 3 Interrupt Vector 14 to 26 - Reserved*	R/W
0x0968	*Module 3 Interrupt Vector 27 – Summary Status*	R/W
0x096C to 0x097C	*Module 3 Interrupt Vector 28 to 32 - Reserved*	R/W

0x0A00	*Module 3 Interrupt Steering 1 - BIT*	R/W
0x0A04	*Module 3 Interrupt Steering 2 - Channel Status Ch 1*	R/W
0x0A08	*Module 3 Interrupt Steering 3 - Channel Status Ch 2*	R/W
0x0A0C	*Module 3 Interrupt Steering 4 - Channel Status Ch 3*	R/W
0x0A10	*Module 3 Interrupt Steering 5 - Channel Status Ch 4*	R/W
0x0A14	*Module 3 Interrupt Steering 6 - Channel Status Ch 5*	R/W
0x0A18	*Module 3 Interrupt Steering 7 - Channel Status Ch 6*	R/W
0x0A1C	*Module 3 Interrupt Steering 8 - Channel Status Ch 7*	R/W
0x0A20	*Module 3 Interrupt Steering 9 - Channel Status Ch 8*	R/W
0x0A24	*Module 3 Interrupt Steering 10 - Channel Status Ch 9*	R/W
0x0A28	*Module 3 Interrupt Steering 11 - Channel Status Ch 10*	R/W
0x0A2C	*Module 3 Interrupt Steering 12 - Channel Status Ch 11*	R/W
0x0A30	*Module 3 Interrupt Steering 13 - Channel Status Ch 12*	R/W
0x0A34 to 0x0A64	*Module 3 Interrupt Steering 14 to 26 - Reserved*	R/W
0x0A68	*Module 3 Interrupt Steering 27 – Summary Status*	R/W
0x0A6C to 0x0A7C	*Module 3 Interrupt Steering 28 to 32 – Reserved*	R/W

0x0B00	*Module 4 Interrupt Vector 1 - BIT*	R/W
0x0B04	*Module 4 Interrupt Vector 2 - Channel Status Ch 1*	R/W
0x0B08	*Module 4 Interrupt Vector 3 – Channel Status Ch 2*	R/W
0x0B0C	*Module 4 Interrupt Vector 4 – Channel Status Ch 3*	R/W
0x0B10	*Module 4 Interrupt Vector 5 – Channel Status Ch 4*	R/W
0x0B14	*Module 4 Interrupt Vector 6 – Channel Status Ch 5*	R/W

0x0C00	*Module 4 Interrupt Steering 1 - BIT*	R/W
0x0C04	*Module 4 Interrupt Steering 2 - Channel Status Ch 1*	R/W
0x0C08	*Module 4 Interrupt Steering 3 - Channel Status Ch 2*	R/W
0x0C0C	*Module 4 Interrupt Steering 4 - Channel Status Ch 3*	R/W
0x0C10	*Module 4 Interrupt Steering 5 - Channel Status Ch 4*	R/W
0x0C14	*Module 4 Interrupt Steering 6 - Channel Status Ch 5*	R/W

0x0B18	*Module 4 Interrupt Vector 7 – Channel Status Ch 6*	R/W
0x0B1C	*Module 4 Interrupt Vector 8 – Channel Status Ch 7*	R/W
0x0B20	*Module 4 Interrupt Vector 9 – Channel Status Ch 8*	R/W
0x0B24	*Module 4 Interrupt Vector 10 – Channel Status Ch 9*	R/W
0x0B28	*Module 4 Interrupt Vector 11 – Channel Status Ch 10*	R/W
0x0B2C	*Module 4 Interrupt Vector 12 – Channel Status Ch 11*	R/W
0x0B30	*Module 4 Interrupt Vector 13 – Channel Status Ch 12*	R/W
0x0B34 to 0x0B64	*Module 4 Interrupt Vector 14 to 26 - Reserved*	R/W
0x0B68	*Module 4 Interrupt Vector 27 – Summary Status*	R/W
0x0B6C to 0x0B7C	*Module 4 Interrupt Vector 28 to 32 - Reserved*	R/W

0x0C18	*Module 4 Interrupt Steering 7 - Channel Status Ch 6*	R/W
0x0C1C	*Module 4 Interrupt Steering 8 - Channel Status Ch 7*	R/W
0x0C20	*Module 4 Interrupt Steering 9 - Channel Status Ch 8*	R/W
0x0C24	*Module 4 Interrupt Steering 10 - Channel Status Ch 9*	R/W
0x0C28	*Module 4 Interrupt Steering 11 - Channel Status Ch 10*	R/W
0x0C2C	*Module 4 Interrupt Steering 12 - Channel Status Ch 11*	R/W
0x0C30	*Module 4 Interrupt Steering 13 - Channel Status Ch 12*	R/W
0x0C34 to 0x0C64	*Module 4 Interrupt Steering 14 to 26 - Reserved*	R/W
0x0C68	*Module 4 Interrupt Steering 27 – Summary Status*	R/W
0x0C6C to 0x0C7C	*Module 4 Interrupt Steering 28 to 32 – Reserved*	R/W

0x0D00	*Module 5 Interrupt Vector 1 - BIT*	R/W
0x0D04	*Module 5 Interrupt Vector 2 - Channel Status Ch 1*	R/W
0x0D08	*Module 5 Interrupt Vector 3 – Channel Status Ch 2*	R/W
0x0D0C	*Module 5 Interrupt Vector 4 – Channel Status Ch 3*	R/W
0x0D10	*Module 5 Interrupt Vector 5 – Channel Status Ch 4*	R/W
0x0D14	*Module 5 Interrupt Vector 6 – Channel Status Ch 5*	R/W
0x0D18	*Module 5 Interrupt Vector 7 – Channel Status Ch 6*	R/W
0x0D1C	*Module 5 Interrupt Vector 8 – Channel Status Ch 7*	R/W
0x0D20	*Module 5 Interrupt Vector 9 – Channel Status Ch 8*	R/W
0x0D24	*Module 5 Interrupt Vector 10 – Channel Status Ch 9*	R/W
0x0D28	*Module 5 Interrupt Vector 11 – Channel Status Ch 10*	R/W
0x0D2C	*Module 5 Interrupt Vector 12 – Channel Status Ch 11*	R/W
0x0D30	*Module 5 Interrupt Vector 13 – Channel Status Ch 12*	R/W
0x0D34 to 0x0D64	*Module 5 Interrupt Vector 14 to 26 – Reserved*	R/W
0x0D68	*Module 5 Interrupt Vector 27 – Summary Status*	R/W
0x0D6C to 0x0D7C	*Module 5 Interrupt Vector 28 to 32 - Reserved*	R/W

0x0E00	*Module 5 Interrupt Steering 1 - BIT*	R/W
0x0E04	*Module 5 Interrupt Steering 2 - Channel Status Ch 1*	R/W
0x0E08	*Module 5 Interrupt Steering 3 - Channel Status Ch 2*	R/W
0x0E0C	*Module 5 Interrupt Steering 4 – Channel Status Ch 3*	R/W
0x0E10	*Module 5 Interrupt Steering 5 - Channel Status Ch 4*	R/W
0x0E14	*Module 5 Interrupt Steering 6 - Channel Status Ch 5*	R/W
0x0E18	*Module 5 Interrupt Steering 7 - Channel Status Ch 6*	R/W
0x0E1C	*Module 5 Interrupt Steering 8 - Channel Status Ch 7*	R/W
0x0E20	*Module 5 Interrupt Steering 9 - Channel Status Ch 8*	R/W
0x0E24	*Module 5 Interrupt Steering 10 - Channel Status Ch 9*	R/W
0x0E28	*Module 5 Interrupt Steering 11 - Channel Status Ch 10*	R/W
0x0E2C	*Module 5 Interrupt Steering 12 - Channel Status Ch 11*	R/W
0x0E30	*Module 5 Interrupt Steering 13 - Channel Status Ch 12*	R/W
0x0E34 to 0x0E64	*Module 5 Interrupt Steering 14 to 26 - Reserved*	R/W
0x0E68	*Module 5 Interrupt Steering 27 – Summary Status*	R/W
0x0E6C to 0x0E7C	*Module 5 Interrupt Steering 28 to 32 – Reserved*	R/W

0x0F00	*Module 6 Interrupt Vector 1 - BIT*	R/W
0x0F04	*Module 6 Interrupt Vector 2 - Channel Status Ch 1*	R/W

0x1000	*Module 6 Interrupt Steering 1 - BIT*	R/W
0x1004	*Module 6 Interrupt Steering 2 - Channel Status Ch 1*	R/W

0x0F08	***Module 6 Interrupt Vector 3 – Channel Status Ch 2***	R/W
0x0F0C	***Module 6 Interrupt Vector 4 – Channel Status Ch 3***	R/W
0x0F10	***Module 6 Interrupt Vector 5 – Channel Status Ch 4***	R/W
0x0F14	***Module 6 Interrupt Vector 6 – Channel Status Ch 5***	R/W
0x0F18	***Module 6 Interrupt Vector 7 – Channel Status Ch 6***	R/W
0x0F1C	***Module 6 Interrupt Vector 8 – Channel Status Ch 7***	R/W
0x0F20	***Module 6 Interrupt Vector 9 – Channel Status Ch 8***	R/W
0x0F24	***Module 6 Interrupt Vector 10 – Channel Status Ch 9***	R/W
0x0F28	***Module 6 Interrupt Vector 11 – Channel Status Ch 10***	R/W
0x0F2C	***Module 6 Interrupt Vector 12 – Channel Status Ch 11***	R/W
0x0F30	***Module 6 Interrupt Vector 13 – Channel Status Ch 12***	R/W
0x0F34 to 0x0F64	***Module 6 Interrupt Vector 14 to 26 – Reserved***	R/W
0x0F68	***Module 6 Interrupt Vector 27 – Summary Status***	R/W
0x0F6C to 0x0F7C	***Module 6 Interrupt Vector 28 to 32 - Reserved***	R/W

0x1008	***Module 6 Interrupt Steering 3 - Channel Status Ch 2***	R/W
0x100C	***Module 6 Interrupt Steering 4 - Channel Status Ch 3***	R/W
0x1010	***Module 6 Interrupt Steering 5 - Channel Status Ch 4***	R/W
0x1014	***Module 6 Interrupt Steering 6 - Channel Status Ch 5***	R/W
0x1018	***Module 6 Interrupt Steering 7 - Channel Status Ch 6***	R/W
0x101C	***Module 6 Interrupt Steering 8 - Channel Status Ch 7***	R/W
0x1020	***Module 6 Interrupt Steering 9 - Channel Status Ch 8***	R/W
0x1024	***Module 6 Interrupt Steering 10 - Channel Status Ch 9***	R/W
0x1028	***Module 6 Interrupt Steering 11 - Channel Status Ch 10***	R/W
0x102C	***Module 6 Interrupt Steering 12 - Channel Status Ch 11***	R/W
0x1030	***Module 6 Interrupt Steering 13 - Channel Status Ch 12***	R/W
0x1034 to 0x1064	***Module 6 Interrupt Steering 14 to 26 - Reserved***	R/W
0x1068	***Module 6 Interrupt Steering 27 – Summary Status***	R/W
0x106C to 0x107C	***Module 6 Interrupt Steering 28 to 32 – Reserved***	R/W

7 ARINC 429/575 Hardware Block Diagram

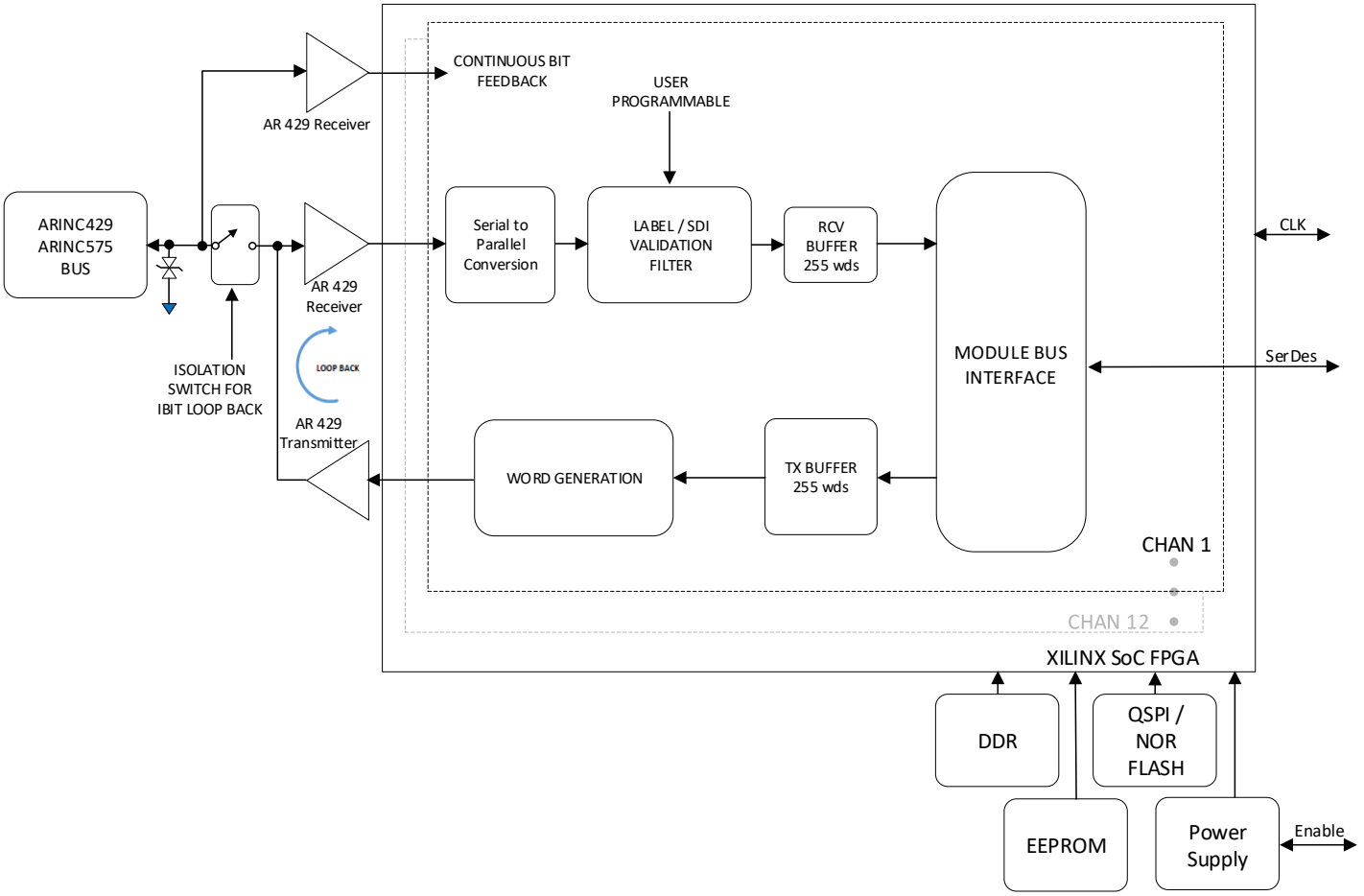


Figure 1 - AR1 Hardware Block Diagram

8 ARINC 429/575 Processing Block Diagram

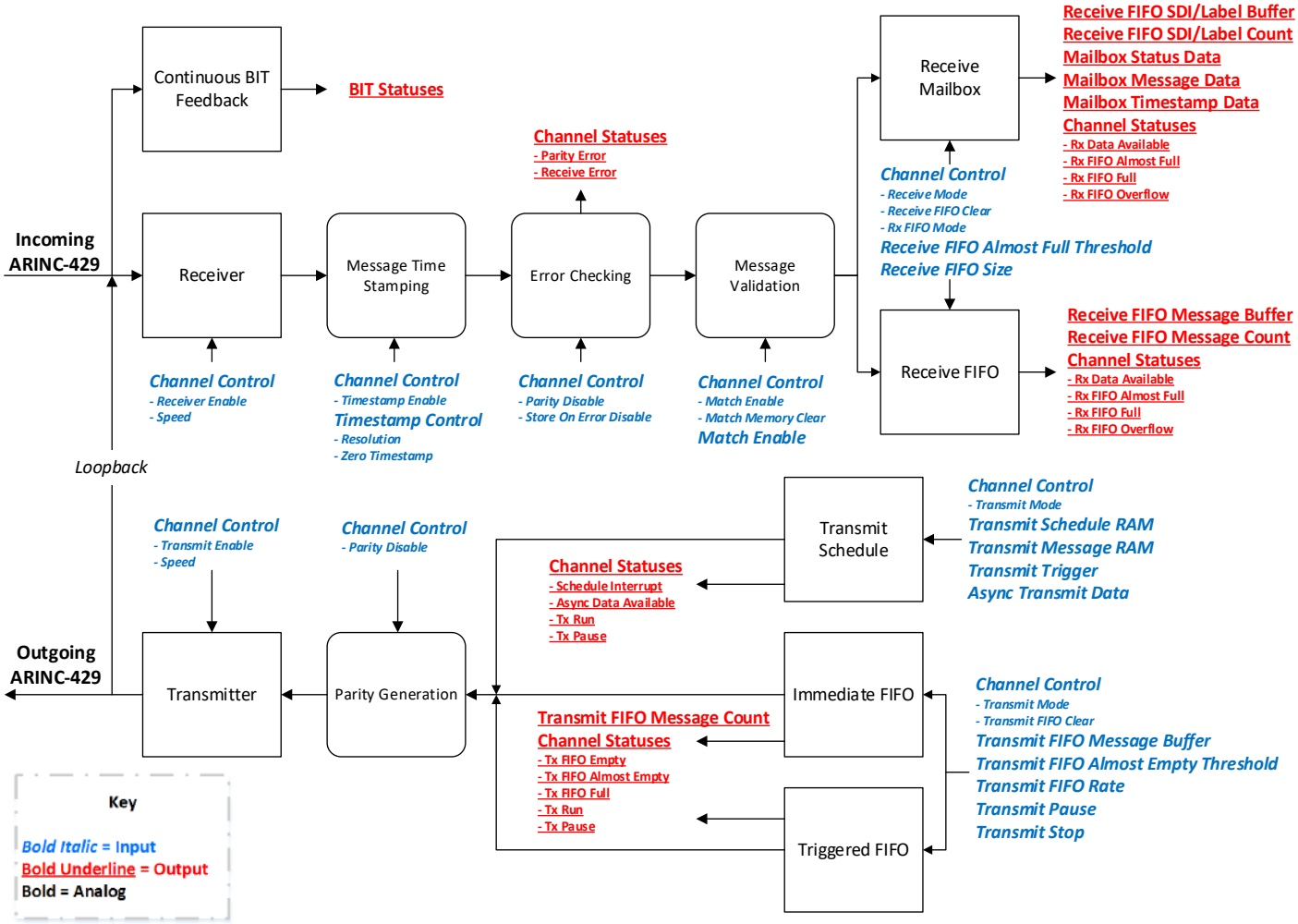


Figure 2 - AR1 Processing Block Diagram

9 Appendix A – Register Name Changes From Previous Releases

This section provides a mapping of the register names used in this document against register names used in previous releases.

Rev B - Register Names	Rev A - Register Names
Receive FIFO Mode Registers	
Receive FIFO Message Buffer	Rx (Receive) Buffer (FIFO)
Receive FIFO Message Count	Rx FIFO (Buffer) Level (Number of Rx Buffer Words)
Receive FIFO Almost Full Threshold	Rx FIFO (Buffer) Threshold
Receive FIFO Size	
Receive Mailbox Mode Registers	
Receive FIFO SDI/Label Buffer	Rx (Receive) Buffer (FIFO)
Receive FIFO SDI/Label Count	Rx FIFO (Buffer) Level (Number of Rx Buffer Words)
Receive FIFO Almost Full Threshold	Rx FIFO (Buffer) Threshold
Receive FIFO Size	
Mailbox Status Data	Mailbox Status Data Register
Mailbox Message Data	Mailbox Message Data Register
Mailbox Timestamp Data	Mailbox TimeStamp Data Register
Timestamp Registers	
Timestamp Control	Timestamp Control Register
Timestamp Value	Timestamp Register
Message Validation Registers	
Match Enable	Mailbox Match Enable Data Register
Transmit FIFO Registers	
Transmit FIFO Message Buffer	Tx (Transmit) Buffer (FIFO)
Transmit FIFO Message Count	Tx FIFO (Buffer) Level (Number of Rx Buffer Words)
Transmit FIFO Almost Empty Threshold	Tx FIFO (Buffer) Threshold
Transmit FIFO Rate	Transmit FIFO Rate
Transmit Scheduling Registers	
Transmit Schedule RAM Command Format	Tx Schedule Program Memory Format
Transmit Message RAM Data Format	
Async Transmit Data	Async Tx Data
Transmit Control Registers	
Transmit Trigger	Transmit Trigger Register
Transmit Pause	Transmit Pause Register
Transmit Stop	Transmit Stop Register
Control Registers	
Channel Control	Channel Control
Module Reset	Module Reset Register
ARINC 429/575 Test Registers	
Test Enabled	
Background BIT Threshold Programming Registers	
Background BIT Threshold	

Reset BIT	
Status and Interrupt Registers	
BIT Dynamic Status	BIT Dynamic Status
BIT Latched Status	BIT Latched Status
BIT Interrupt Enable	BIT Interrupt Enable
BIT Set Edge/Level Interrupt	BIT Set Edge/Level Interrupt
Channel Dynamic Status	Dynamic Status
Channel Latched Status	Latched Status
Channel Interrupt Enable	Interrupt Enable
Channel Set Edge/Level Interrupt	Set Edge/Level Interrupt
Summary Dynamic Status	
Summary Latched Status	
Summary Interrupt Enable	
Summary Set Edge/Level Interrupt	

10 Firmware Revision Notes

This section identifies the firmware revision in which specific features were released. Prior revisions of the firmware would not support the features listed.

Feature	FPGA		Bare Metal (BM)	
	Firmware Revision	Release Date	Firmware Revision	Release Date
Background BIT Threshold Programming	1.00022	9/18/2019 4:23:29 PM	2.3	1/10/2020 11:05:30 AM
Test Enabled	1.00022	9/18/2019 4:23:29 PM	2.3	1/10/2020 11:05:30 AM
Summary Status	1.00022	9/18/2019 4:23:29 PM	2.3	1/10/2020 11:05:30 AM

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