Accelerate Your Time-to-Mission™

Serial Communications
SC1, SC7 & SC2
Function Modules

MODULE MANUAL

Revision History

Revision	Revision Date	Description	Author
A	2/1/2018	Initial release	SL
A1	2/21/2018	ECO C05374, clarification of various technical data	SL
A2	3/5/2018	ECO C05412, updates to module manual consistency	SL
A3	3/28/2018	ECO C05470, added gap timeout feature renamed manual to Module Manual - SC1, SC7 & SC2	SL

Table of Contents

Introduction

This module manual provides information about the North Atlantic Industries, Inc. (NAI) Serial Communications Function Module: SC1, 2 and 7. These modules are compatible with all NAI Generation 5 motherboards.

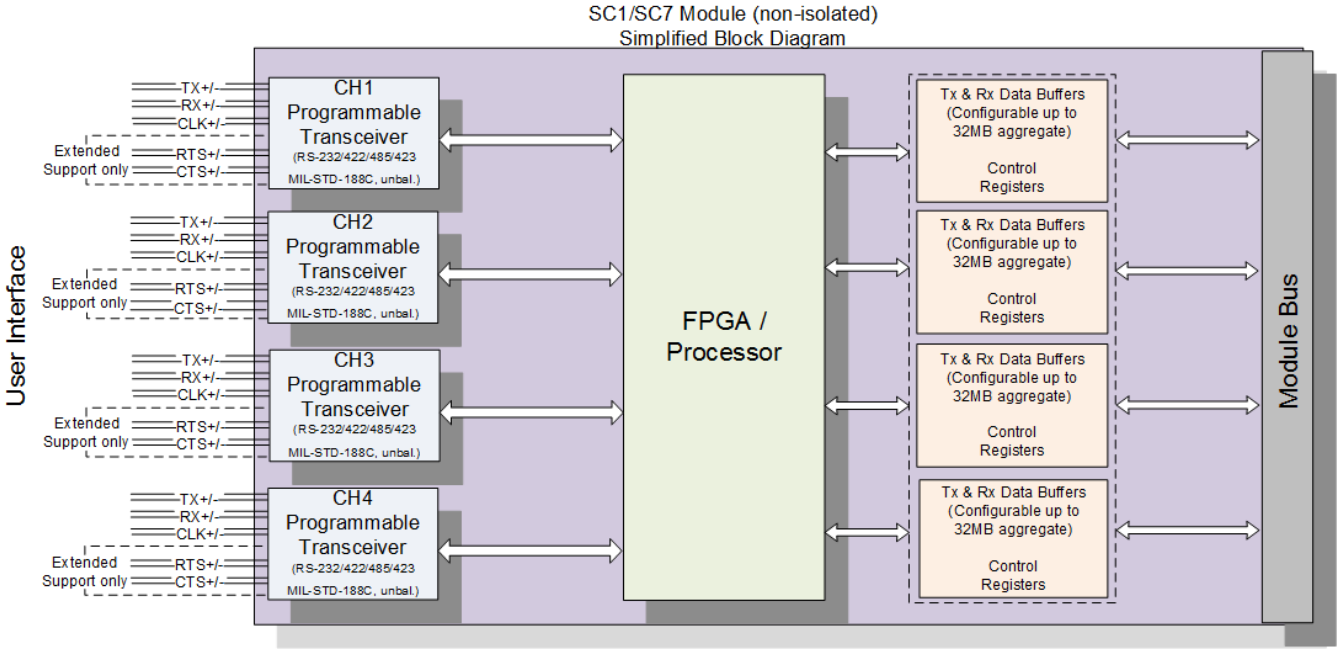
Serial Communications Modules SC1, SC2 and SC7 support four intelligent, full-duplex, independent, multi-channels that can be individually software-configured for RS-232C, RS-422, RS-423 (Pending), and RS-485 communications. They also provide MIL-STD-188C unbalanced interface support, with data and/or clock bit inversion and synchronous or asynchronous communications. These capabilities make them the perfect choice for many new and legacy communication applications. SC1 provides non-isolated outputs. SC2 provides isolated outputs. SC7 is the same as SC1 except SC7 reallocates the pins used for CTS Flow Control as four (4) additional system grounds.

Features

- Each channel can be programmed into a Loop-Back mode that internally wraps the transmitter around the receiver without the need of external wiring.
- An additional asynchronous mode to support “Immediate Transmit” operation results in Serial Data Transmit Enhancement. Each channel has its own Transmit and Receive buffer where total aggregate buffer allocation is user configurable/programmable up to 64 MB.
- A Receiver Enable/Disable function allows the user to turn selected receivers ON/OFF.
- This serial card can operate in an Interrupt-Driven Environment to provide notification of all events to the system. When a flow control mode is selected, the serial card does the operation automatically with minimal system intervention.
- Multi-Drop Link Mode: The transmitter and receivers of up to 32 cards can be tied together in either Half or Full-Duplex mode.
- Built-in Test

Specifications

Module SC1/SC7 - Serial Communications with Programmable Interface Levels



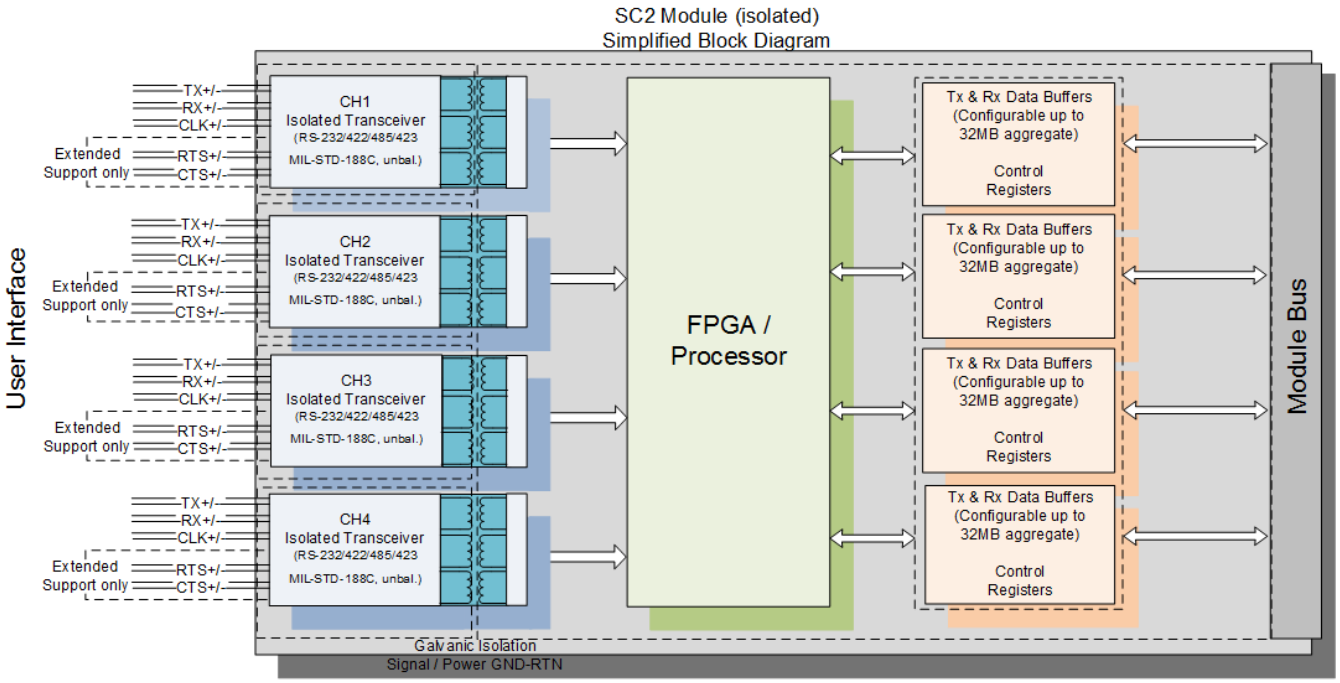
Number of Channels:	Four (4) high-speed, fully programmable RS-232, RS-422, RS-485, RS-423(Pending w/ MIL-STD-188C unbalanced support), non-isolated
Data Rate: **(per channel, unless otherwise specified)**	10 (5) Mbps: SYNC/HDLC (if Manchester encoded), RS-422/485 1.5 Mbps: ASYNC, RS-422/485 250 Kbps: RS-232/423 or MIL-STD-188C unbalanced Data rate will be within 1% of commanded rate. Data can be read 4 µs after receipt in UART*. These data rates are verified with all channels running simultaneously*.
Data Transfer:	Data transfers within 300 ns, no latency issues*.
Receive/Transmit Buffers:	Configurable Receive and Transmit buffers (up to 32 MB, aggregate). Accessed in 16-bit mode only.
Power:	5 VDC @ 350 mA per module (typ./est.) / Signals are non-isolated (referenced to system/power GND).
Weight:	1.5 oz. (42 g)

* Pending qualification.

Note: SC7 is exactly the same as SC1 except SC7 reallocates the pins used for CTS Flow Control as four (4) additional system grounds.

Specifications are subject to change without notice.

Module SC2 – Isolated Serial Communications with Programmable Interface Levels



Number of Channels:	Four (4) high-speed, fully programmable RS-232, RS-422, RS-485, RS-423 (Pending w/ MIL-STD-188C unbalanced support), isolated
Data Rate:	10 Mbit/s per channel in Synchronous/HDLC mode 1 Mbit/s per channel in Asynchronous mode (RS-422 & RS-485) 250 Kb/s RS-423 (Pending), MIL-STD-188C unbalanced Data rate will be within 1% of commanded rate. Data can be read 4 µs after receipt in UART*. These data rates are verified with all channels running simultaneously.*
Data Transfer:	Data transfers within 300 ns, no latency issues*.
Receive/Transmit Buffers:	Configurable Receive and Transmit buffers (up to 32 MB, aggregate). Accessed in 16-bit mode only.
Power:	5 VDC @ 350 mA per module (typ./est.) / Signals are isolated (not referenced to system/power GND).
Weight:	1.5 oz. (42 g)

* Pending qualification.

Specifications are subject to change without notice.

Principle of Operation

The module can be individually software configured for RS-232C, RS-422, RS-485, or RS-423 (Pending), Synchronous or Asynchronous Communication. Additional support for MIL-STD-188C section 7.2.1 prior to Notice 1 hardware interface level functionality, as well as support for bit polarity inversion capability on TxD, RxD and CLK is also provided. The architecture avoids latency problems because all data transfer is done in hardware and not in software. Any incoming data, no matter how many channels are active, in whatever mode, can be immediately extracted. A BREAK sequence capability is also incorporated. FPGA design simplifies programming and usage.

Note: Due to pin count constraints, extended handshaking capability is not supported.

Internal Loop Back Self-Test

Internal Loop Back Self-Test is performed when power is applied, and results are stored in registers. During Loop Back test, the outputs are disconnected. Each channel can be programmed into a Loop Back mode that internally wraps the transmitter around the receiver without the need of external wiring. Output short circuit capability is continuous and bulletproof. If the card is not powered, neither the inputs nor outputs will load down the lines. Inputs and outputs can withstand ±15 volts under any condition. All serial lines are transient and protected to IEC1000 4-2, 4-4, & 4-5.

Built-In Test

The module provides a user initiated Built-in-Test (BIT) for each channel. It is set using the *Tx-Rx Configuration* register. To run BIT, ensure the selected channel is disabled by writing a **0** to the ENABLE CHANNEL bit, D24 in the *Tx-Rx Configuration* register. BIT will not run if the channel is enabled. Start BIT by writing a **1** to the INITIATE BIT, D27 in the *Tx-Rx Configuration* register. Wait 5 ms and check D27 for **0**, which indicates that BIT testing is complete. If you do not read **0** after 5 ms, then BIT has timed out because it did not execute or did not finish executing. In either case, the result is inconclusive. If **0** is read from D27 of the *Tx-Rx Configuration* register, then BIT has completed and the results are provided by the *BIT Status* registers (real-time or latched). The BIT status registers are bitmapped channel-wise, meaning D0 is the BIT result of channel 1, D1 is the BIT result of channel 2, D2 is the BIT result of channel 3, etc. A **0** indicates that the channel passed; a **1** indicates that it failed.

Serial Data Transmit Enhancement

An additional asynchronous mode to support “Immediate Transmit” operation has been incorporated. This mode immediately transmits serial data anytime the transmit buffer is not empty. There is no requirement to set the “Tx Initiate” bit after each byte, which simplifies system traffic and overhead, since only the actual data byte being transmitted needs be sent to the transmit buffer. Each channel has its own configurable Transmit and Receive buffer. While in Asynchronous mode, the upper byte of each received word provides status information for that word.

Receiver Enable/Disable

A Receiver Enable/Disable function allows the user to turn selected receivers ON/OFF. When a receiver is disabled, no data will be placed in the buffer. CRC code generation and detection is also available for message integrity when used in Synchronous and HDLC modes.

Interrupts

This serial card can operate in an Interrupt Driven Environment to provide notification of all events to the system. It supports hardware flow control (CTS/RTS) as well as software flow control (XON, XOFF). When a flow control mode is selected, the serial card does the operation automatically with minimal system intervention. A Parity Error Interrupt is provided for each byte throughout the communications data stream.

Multi-Drop Link Mode (RS485)

The transmitter and receivers of up to 32 channels can be tied together in either Half or Full-Duplex mode. While in Multi-Drop Link Mode, the transmit line for each channel will automatically change from tri-state mode to enable and transmit any data as soon as it is placed in the transmit buffer. Once transmission is completed, the transmit line is automatically changed back to tri-state mode.

To program a SCx serial channel for Multi-Drop mode, the interface level must be set to (RS485), and the Tristate transmit line (bit) in the channel control register must be set.

CTS/RTS and GPIO/GND

Module SC1 provides Flow Control mode. The Request to Send (RTS) output and Clear to Send (CTS) input are available only on SC1. Note that extended support from the factory is necessary for access to Flow Control mode through the rear connector. SC2 does not provide Flow Control mode. For SC2, a channel ground (GND) and a general-purpose output (GP-Out) are provided. SC7 also does not provide Flow Control mode. For SC7, four additional System Ground pins are provided.

Serial Communications Specifications

Specifications	RS-232	RS-422	RS-485	RS-423(Pending)/ MIL-STD-188C
Mode of Operation:	Single Ended	Differential	Differential	Single Ended
Total number of Drivers & Receivers on one line:	1 driver, 1 receiver	1 driver, 1 receiver	1 driver, 32 receivers	1 driver, 1 receiver
Maximum Data Rate:	120 kb/s	1M b/s Asynch 10 Mb/s Synch	1 Mb/s Asynch 10 Mb/s Synch	250 Kb/s
Driver Output Signal Level (Min Loaded):	±5V @3kΩ load	±2.0V@100Ω load	±1.5V@54Ω load	±6V ±1V@ ≥ 6KΩ load
Driver Load Impedance (Ohms):	3k min	100	54	> 6KΩ
Max. Driver Current in High Z State (Power On):	N/A	N/A	±100uA	N/A
Max. Driver Current in High Z State (Power Off):	±6mA@±2V	±100uA	±100uA	±100uA
Receiver Input Voltage Range:	±15V	-10V to +10V	-7V to +12V	-7V to +7V
Receiver Input Sensitivity:	±3V	±200mV	±200mV	±2V
Receiver Input Resistance (Ohms):	3k to 7k	120	10k	6k

Note: The EIA232 standard uses negative, bipolar logic in which a negative voltage signal represents logic **1**, and positive voltage represents logic **0**.

Communication Module Factory Defaults: Registers and Delays

Address Recognition:	Off
Baud Rate:	9600
CTS/RTS:	Disabled
Protocol:	0, Asynchronous
Clock Select:	Internal
Clock Mode:	0
Interface Levels:	5
HDLC Rx Address/Sync Character:	0x00A5h
HDLC Tx Address/Sync Character:	0x00A5h
Termination Character:	0x0003h
Interrupt Level:	0
Interrupt Vector:	0x00
Mode:	Tri-State, asynchronous
Number of Data Bits:	8
Parity:	Disabled
Receivers:	Disabled
Number of Words TX Buffer:	0
Number of Words Rx Buffer:	0
Rx Buffer, Almost Full:	0x1FFF9B
Stop Bits:	1
Tx Buffer, Almost Empty:	0x0064h
Tx-Rx Configuration High:	0
Tx-Rx Configuration Low:	0
Channel Control High:	0
Channel Control Low:	0
Channel Control Extended:	0
Data Configuration:	0x0108
Preamble:	0
Rx Buffer High Watermark:	0x1FFF9B
Rx Buffer Low Watermark:	0x0800h
XON:	0x0011h
XOFF:	0x0013h
XON/XOFF:	Disabled
Time Out Value:	0x9C40h

A write to the following registers takes place immediately:

Transmit Data
Channel Control
Interrupt Enable
Clear Interrupt
Set Interrupt Edge/Level

For all other registers, Channel configure protocol must be followed.

Register Descriptions

The register descriptions provide the register name, Register Offset, Type, Data Range, Read or Write information, Initialized Value, a description of the function and, in most cases, a data table.

Transmit Buffer

Function: Data intended to be transmitted is placed in this buffer prior to transmission.

Type: unsigned character word

Data Range: 0x0000 0000 to 0x FFFF FFFF

Read/Write: W

Initialized Value: Not Applicable (NA)

Operational Settings: Data words are 8-bit and occupy the register's lowest significant bits (LSBs), or low byte.

Transmit Buffer																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	**D[1]**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	X=DON'T CARE, D=DATA BIT

- Data only in Asynchronous 9-bit mode

Receive Buffer

Function: Received data is placed in this buffer.
Type: unsigned integer word.
Data Range: 0x0000 0000 to 0x FFFF FFFF
Read/Write: R
Initialized Value: NA
Operational Settings: Data is received in the low byte as unsigned integer. The high byte is used for status.

Receive Buffer																	
REGISTER	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
	S	**S**	**S**	**S**	**S**	**S**	**S**	**S**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	S=STATUS BIT, D=DATA BIT
Asynchronous	**PE**	**FE**	**OE**	X	X	**EOF**	**P**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	EOF only if Termination Char is used
Bi/Mono Synchronous	X	X	X	X	X	**ERR**	**EOF**	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	
HDLC Mode	X	**BOF**	X	**ER2**	**ER1**	**ER0**	**EOF**	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	Last Word is Status Word

PE	= Parity Error	'1' Calculated parity does not match the received parity bit
FE	= Framing Error	'1' A character framing error was detected.
OE	= Overrun Error	'1' A character was received while the FIFO was full
BOF	= Beginning Of Frame	'1' Indicates first character of frame. Useful to identify multiple frames in large buffer.
EOF	= End Of Frame	'1' Indicates End of Frame. Useful to identify multiple frames in large buffer.
P	= Parity Bit	This bit carries the Parity bit of the last received character
ER2..0:		HDLC Error Code:
		000 = Good Frame
		111 = CRC Error
		001 = Frame Aborted

Number of Words Tx Buffer

Function: Contains the number of words to be transmitted.
Type: unsigned integer
Data Range: 0x0000 0000 to 0x 0x2000000
Read/Write: R
Initialized Value: 0
Operational Settings: Reads Integers

Number of Words Tx Buffer																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Number of Words Rx Buffer

Function: Contains the number of words received.

Type: unsigned integer

Data Range: 0x0000 0000 to 0x2000000

Read/Write: R

Initialized Value: 0

Operational Settings: Reads Integers

Number of Words Rx Buffer																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Protocol

Function: Configures the associated channel for either asynchronous, mono-synchronous, bi-synchronous, or HDLC mode.

Type: unsigned integer

Data Range: NA

Read/Write: W

Initialized Value: 0, Asynchronous

Operational Settings: See table below.

Protocol																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	ASYNC
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	MONO-SYNC
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	BI-SYNC
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	HDLC

Clock Mode

Function: Configures clock for internal (driven) or external (received) transmit/receive clocks
Type: unsigned integer
Data Range: NA
Read/Write: W
Initialized Value: 0
Operational Settings: Applicable only for Sync or HDLC as set by *Protocol* register.

Clock Mode																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	Internal
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	External
0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	INVERT Tx Clock
0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	INVERT Rx Clock

Interface Levels

Function: Configures the interface level (RS-232, RS-422, RS-423 (Pending), RS-485, Loop Back, or Tri-State) for the associated channel.

Type: unsigned integer

Data Range: NA

Read/Write: W

Initialized Value: 5

Operational Settings: Loop Back selection connects the channel's transmit and receive line internally. To implement, user must send data and look at Receive FIFO to verify that the sent data. Loop Back is usually used for test.

Note: Synchronous modes (mono-synchronous, bi-synchronous, or HDLC mode) should not be put in manual loopback or FPGA loopback mode. Synchronous modes are designed to have one channel drive the clock and one channel receive the clock. In loopback modes, the internal clock will be used for both Tx and Rx. While this may work, it is not recommended or reliable. If two channels are wired to each other for external loopback, then the clock must be inverted.

Interface Levels																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	RS232
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	RS422
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	**0**	RS423*
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	RS485
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**0**	MANUAL LOOP BACK
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**1**	TRI-STATE
0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	FPGA LOOP BACK

* MIL-STD-188C hardware interface levels enabled by setting RS-423 (Pending), bit and use of Tx/Rx Data inversion as/if required.

Tx-Rx Configuration

Function: Sets the transmit/receive configuration for the associated channel.

Type: binary word

Data Range: NA

Read/Write: R/W

Initialized Value: 0

Operational Settings: Functions depend upon programmed protocol (see *Protocol* Register).

Lower Bits - Bits D0 through D15 of this register are used to configure CRC function and OPEN and IDLE flags. In HDLC mode, error protection is done by CRC generation and checking. The frame sequence at the end of each frame consists of two or four bytes of CRC checksum. 32-bit or CCITT algorithms may be selected.

Upper Bits - Bits D16 through D31 of this register are used to set the transmit/receive configuration for the associated channel. Functions depend upon programmed protocol (see Protocol Register).

BIT - Set ENABLE CHANNEL bit, D24 low (**0**) to clear the selected channel. Set INITIATE BIT D27 high (**1**) to initiate BIT. After 5 ms, a **0** should be read**,** which indicates that the BIT test is complete. The *BIT Status* register reports the channel status.

Tx-Rx Configuration Upper Bits (Hi)																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	RTS Invert. 0=Normal, 1=Invert
0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	CTS Invert. 0=Normal, 1=Invert
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	CRC RESET VALUE 1=0's / 0=1's
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	0	16-BIT CRC (SYNC ONLY)
0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	0	32-BIT CRC (HDLC ONLY)
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	0	16-BIT CCITT
0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	1=APPEND CRC TO Tx DATA, EXPECT CRC WITH Rx DATA, 0=no CRC
0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	IDLE FLAG (0x7E) TRANSMISSION*
0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	Rx SUPPRESSION 0=RECEIVER ALWAYS ON 1=RECEIVER OFF DURING TRANSMISSION
0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	INVERT CTS
0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	INVERT RTS
0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	ENABLE CHANNEL
0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	INITIATE BIT
0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	ENABLE GAP TIMEOUT**

* Idle Flag (0x7E) Transmission and Reception functionality is pending. Currently not supported. Idle Flag functionality once implemented will provide the following: During idle times when no frames are being transmitted, the SC1/SC2/SC7 will transmit idle flag (0xFF). The SC1/SC2/SC7 expects idle flag (0xFF) to be sent during idle times when no frames are being transmitted. Transmission of 0x7E idle flags during this time will result in an error condition.
** Gap Timeout feature available as of FPGA revision 25, DOM 4/6/2018.

Tx-Rx Configuration Lower Bits (Lo)																
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RTS/CTS FLOW CONTROL
0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx ADDRESS RECOGNITION (HDLC ONLY)
0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Tx ADDRESS TRANSMISSION (HDLC ONLY)
0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	ADDRESS RECOGNITION (HDLC ONLY)
0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	ADDRESS LENGTH (HDLC ONLY) 1=16 / 0=8 BITS
0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SYNC CHAR LENGTH 1=(8)MONO,(16)BiSync 0=(6)MONO,(12)BiSync
0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR AS DATA 1=KEPT / 0=STRIPPED
0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	TERMINATION CHAR DETECTION
0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	XON/XOFF FLOW CONTROL
0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	XON/XOFF CHAR AS DATA 1=KEPT / 0=STRIPPED
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TIME OUT DETECTION

Notes: To use RTC/CTS functions as GPIO set the RTS/CTS FLOW CONTROL **D0** to 0. To change the state of RTS output write a **1** or **0** to bit **D0** in the *Channel Control* register for RTS/GPIO. For monitoring the RTS/CTS functions as GPIO it is recommended to use the *Latched Status* register.

Channel Control

Function: Channel control configuration.
Type: binary word
Data Range: NA
Read/Write: R/W
Initialized Value: 0
Operational Settings: Real time control of the Serial channel.

Channel Control																	
REGISTER	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
CONTROL HI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	Tx INITIATE[3]
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Tx ALWAYS (ASYNC ONLY)
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	ENABLE RECEIVER
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
CONTROL LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RTS/GPIO 1[1]
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	TRISTATE TRANSMIT LINE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SET/RELEASE BREAK
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET CHANNEL FIFOs & UART
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLEAR Rx FIFO[2]
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLEAR Tx FIFO[2]

Notes: 1. RTS/CTS as GPIO when RTS/CTS Flow Control disabled.
2. BIT is self-clearing.
3. BIT is cleared when all data from the Tx Buffer is transmitted.
4. To program for Multi-Drop Mode, the interface level must be set to RS485 and the Tristate Transmit line **D0** must be set.

Data Configuration

Function: Channel data configuration.
Type: binary word
Data Range: NA
Read/Write: R/W
Initialized Value: 0
Operational Settings: Sets up the Serial channel configuration.

Data Configuration																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	**N**	**N**	**N**	**N**	NUM OF DATA BITS*
0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	0	0	0	0	NO PARITY
0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	0	0	0	0	SPACE PARITY
0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	0	0	0	0	ODD PARITY
0	0	0	0	0	0	0	0	0	**1**	**0**	**1**	0	0	0	0	EVEN PARITY
0	0	0	0	0	0	0	0	0	**1**	**1**	**1**	0	0	0	0	MARK PARITY
0	0	0	0	0	0	**0**	**1**	0	0	0	0	0	0	0	0	1 STOP BIT
0	0	0	0	0	0	**1**	**0**	0	0	0	0	0	0	0	0	2 STOP BITS
0	**0**	**0**	**0**	0	0	0	0	0	0	0	0	0	0	0	0	NO ENCODING
0	**1**	**1**	**0**	0	0	0	0	0	0	0	0	0	0	0	0	MANCHESTER (GE Thomas)
0	**1**	**1**	**1**	0	0	0	0	0	0	0	0	0	0	0	0	MANCHESTER (IEEE 802.3)

* N=actual number of data bits. Asynchronous: 5-9; Synchronous: 8.

* NO ENCODING is NRZ Data Encoding by default.

Baud Rate

Function: Sets the baud rate for communications.

Type: 24-bit unsigned integer

Data Range: 300 to 10 Mbps Sync (1Mbps Async), Baud Rate High & Low Registers combined

Read/Write: R/W

Initialized Value: 9600 Baud

Operational Settings: Both the Baud Rate High Register and Baud Rate Low Register are combined to determine the communications baud rate. Enter the desired baud rate directly as 24-bit unsigned integer.

Baud Rate High Register																Baud Rate Low Register															
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Preamble

Function: Determines both the number of preambles and the preamble pattern sent out during preamble transmission.

Type: binary word

Data Range: Up to “n” preambles (value 0xDD)

Read/Write: R/W

Initialized Value: 0

Operational Settings: The high byte indicates the number of preambles. The low byte describes the preamble pattern. Preamble transmission applies to both the HDLC and Sync modes. In HDLC-mode, zero-bit insertion is disabled during preamble transmission. Affected Modes: HDLC, Bi-Sync.

Preamble																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON’T CARE, D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
N	N	N	N	0	0	0	0	D	D	D	D	D	D	D	D	N PREAMBLES (VALUE 0xDD)

Tx Buffer Almost Empty

Function: Specifies the minimum size, in bytes, of the transmit buffer before the TxFIFO Almost Empty Status bit D1 in the *FIFO Status* register is flagged (High True).

Type: unsigned integer

Data Range: 0 to Buffer Size

Read/Write: R/W

Initialized Value: 100 decimal (64h)

Operational Settings: If the interrupt is enabled (see *Interrupt Enable* register), a System interrupt will be generated.

Tx Buffer Almost Empty																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer Almost Full

Function: Specifies the maximum size, in bytes, of the receive buffer before the RxFIFO Almost Full Status bit D0 in the *FIFO Status* register is flagged (High True).

Type: unsigned integer

Data Range: 0 to Buffer Size

Read/Write: R/W

Initialized Value: 2097051 (0x1FFF9B)

Operational Settings: If the interrupt is enabled (see *Interrupt Enable* register), a System interrupt will be generated.

Rx Buffer Almost Full																
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer High Watermark

Function: Defines the Receive Buffer High Watermark value.

Type: binary word

Data Range: Low Watermark < High Watermark < 0x1FFF9B

Read/Write: R/W

Initialized Value: 2097051 (0x1FFF9B)

Operational Settings: When Rx Buffer size equals the High Watermark value, FIFO Status bit D3 is flagged and:

- If XON/XOFF is enabled, XOFF is sent, and/or
- If RTS/CTS is enabled, RTS goes inactive.

The Watermark registers are used for XON/XOFF and/or RTS/CTS flow control. The *Receive Buffer High Watermark* register value controls when the XOFF character is sent when using software flow control and controls when the RTS signal would be negated when using hardware flow control.

For software flow control operation, the XOFF character would be sent once when the number of bytes in the Rx FIFO equals the value in the *Receive Buffer High Watermark* register. Once the XOFF has been sent, it cannot be sent again until the XON character has been sent. The valid state transitions to sending the XOFF character can be either no previous XON/XOFF character sent or a previous XON character sent.

There is also a High Watermark Reached interrupt enable/ disable bit in the *Interrupt Enable* register and a High Watermark Reached bit in the ISR, (*Interrupt Status* Register). When the High Watermark is reached, an interrupt request will be generated, when the interrupt enable/disable bit is enabled.

Rx Buffer High Watermark																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Rx Buffer Low Watermark

Function: Defines the Receive Buffer Low Watermark value.

Type: binary word

Data Range: 0 < Low Watermark < High Watermark < 0x1FFF9B

Read/Write: R/W

Initialized Value: 2048 decimal (800h)

When the Rx Buffer size is less than the Low Watermark value, FIFO Status bit D3 is flagged.

- If XON/XOFF is enabled, XON is sent, and/or
- If RTS/CTS is enabled, RTS goes active

The Watermark registers are used for XON/XOFF and/or RTS/CTS flow control. The *Receive Buffer Low Watermark* register value controls when the XON character is sent when using software flow control and controls when the RTS signal would be asserted when using hardware flow control.

For software flow control operation, the XON character would be sent once when the number of bytes in the Rx FIFO equals the value in the *Receive Buffer Low Watermark* register AND an XOFF character has been sent prior to this XON character. The valid state transition to sending the XON character can only be from the state of a previous XOFF character that has been sent.

There is a Low Watermark Reached interrupt enable/disable bit in the *Interrupt Enable* register and a Low Watermark Reached bit in the ISR, (*Interrupt Status* register). When the Low Watermark is reached, an interrupt request will be generated, when the interrupt enable/disable bit is enabled.

Rx Buffer Low Watermark																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

HDLC Rx Address/Sync Character

Function: Mode dependent for HDLC and Synchronous modes. See Operational Settings.

Type: unsigned character word

Data Range: NA

Read/Write: R/W

Initialized Value: A5h

Operational Settings: If using HDLC mode, this value is compared to the address of the received message and if it's equal, the message is stored in the receive buffer. If using Mono/Bi-Synchronous mode, this value is considered the "Sync Character" and is used for communication synchronization. The receiver searches incoming data for the Sync Character. Once found, communication is synchronized and additional data is valid. When in 16-bit, high byte is sent before low byte. Modes Affected: HDLC and Synchronous.

HDLC Rx Address/Sync Character																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

HDLC Tx Address/Sync Character

Function: Mode dependent for HDLC and Synchronous modes. See Operational Settings.

Type: unsigned character

Data Range: NA

Read/Write: R/W

Initialized Value: A5h

Operational Settings: If using HDLC mode, this value is compared to the address of the received message and if it's equal, the message is stored in the receive buffer. If using Mono/Bi-Synchronous mode, this value is considered the "Sync Character" and is used for communication synchronization. The receiver searches incoming data for the Sync Character. Once found, communication is synchronized and additional data is valid. When in 16-bit, high byte is sent before low byte. Modes Affected: HDLC and Synchronous.

HDLC Tx Address/Sync Character																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

XON Character

Function: Specifies the XON character for in-band flow control in Async mode.
Type: unsigned character (usually a member of the ASCII data set)
Data Range: NA
Read/Write: R/W
Initialized Value: 11h
Modes Affected: Async
Operational Settings: When software flow control is enabled, this value is sent as the XON character.

XON Character																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

XOFF Character

Function: Specifies the XOFF character for in-band flow control in Async mode.
Type: unsigned character (usually a member of the ASCII data set)
Data Range: NA
Read/Write: R/W
Initialized Value: 13h
Modes Affected: Async
Operational Settings: When software flow control is enabled, this value is sent as the XOFF character.

XOFF Character																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Termination Character

Function: Contains the termination character used for termination detection.
Type: unsigned character (usually a member of the ASCII data set)
Data Range: NA
Read/Write: R/W
Initialized Value: 3h
Operational Settings: When using the Asynchronous or Bi-Synchronous modes, the receive data stream is monitored for the occurrence of the termination character. When this character is detected, an interrupt is generated, if enabled and not masked. Modes Affected: Async and Sync.

Termination Character																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Time Out Value

Function: Determines the timeout period.
Type: unsigned integer
Data Range: 0 to 65535
Read/Write: R/W
Initialized Value: 9C40h (1 second)
Operational Settings: If there is no receive line activity for the configured period of time, a timeout is indicated in the *Interrupt Status* register, bit D10. LSB is 25µs. Modes Affected: Async.

Time Out Value																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Status and Interrupt Registers

The registers may be set for any or all channels and will latch if a transition is detected on a channel or channels. Each channel(s) will remain latched until the channel is cleared. Multiple channels may be cleared simultaneously, if desired. Each channel bit in the register is polled for a read status. Any subsequent channel(s) transition, if detected, will propagate through to be read (rolling-latch).

Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel) location (bit mapped per channel), will "clear" the bit (set the bit to **0**) if the actual interruptible event condition has cleared. If the interruptible condition "event" is still persistent while clearing, this may retrigger the interrupt.

There is a corresponding Interrupt Enable and vector associated with each "Latched" Status. Each status type may be "polled" (at any time), or is "interruptible" when interrupts are enabled and the associated Interrupt Service Routine (ISR) vectors are programmed accordingly. When programmed for "interruptible" status, interrupts are typically generated and flagged with the programmed vector available as data. The host or single board computer (SBC) typically services the interrupt by a general or specific ISR, which reads the (typically) unique programmed vector (identifier of which status generated the interrupt), reads the associated status register to determine which channel in the status register was "flagged" and then "clears" the status register. This essentially resets the interrupt mechanism, which is now ready to be triggered by the next status register detected event "flag". "Latched Status" will trigger on either "sense on edge" or "sense on level" based on the settings of the associated Set Edge/Level Interrupt register. Sense on "edge" requires a change from low to high state to trigger the status detection, while sense on "level" is independent of the previous state. Unless otherwise specified, all status or fault indications are bit set per channel.

BIT Dynamic Status

Function: Checks the corresponding bit for a channel's BIT Status in real time.

Type: 32-bit unsigned integer

Data Range: 0x0000 0000 to 0x0000 00FF

Read/Write: R

Initialized Value: 0

Operational Settings: 0 = Normal; **1** = Non-functional Serial Loopback. BIT is initiated by the user for serial communications modules.

BIT Dynamic Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Latched Status

Function: Checks the corresponding bit for a channel's BIT Status. Latches status until reset.

Type: 32-bit unsigned integer

Data Range: 0x 0000 0000 to 0x 0000 00FF

Read/Write: R/W

Initialized Value: 0

Operational Settings: 0 = Normal; **1** = Non-functional Serial Loopback. Write **1** to reset the register. BIT is initiated by the user for serial communications modules

BIT Latched Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Interrupt Enable

Function: Generates an interrupt when *BIT Dynamic Status* or *BIT Latched Status* registers indicate a fault condition. Interrupt #1.

Type: 32-bit unsigned integer

Data Range: 0x0000 0000 to 0x0000 00FF

Read/Write: R/W

Initialized Value: 0

Operational Settings: 0 = Disabled; **1** = Enabled.

BIT Interrupt Enable															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

BIT Set Edge/Level Interrupt

Function: Selects whether BIT Interrupt Enable will initiate on a rising edge or level.
Type: 32-bit unsigned integer
Data Range: 0x0000 0000 to 0x0000 00FF
Read/Write: R/W
Initialized Value: 0
Operational Settings: 0 = Rising Edge; **1** = Level.

BIT Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
X	X	X	X	X	X	X	X	X	X	X	X	Ch.4	Ch.3	Ch.2	Ch.1

FIFO Status

Function: Describes current FIFO Status.
Type: binary word
Data Range: NA
Read/Write: R
Initialized Value: NA
Operational Settings: See *Rx Almost Full*, *Tx Almost Empty*, *Rx High Watermark* and *Rx Low Watermark* specific registers for function description and programming.

FIFO Status																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X=DON'T CARE, D=DATA BIT
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RxFIFO ALMOST FULL
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	TxFIFO ALMOST EMPTY
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	HIGH WATERMARK REACHED
0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	LOW WATERMARK REACHED
0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx EMPTY
0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Tx FULL

Dynamic Status

Function: Describes the status of 15 different events.

Type: binary word

Data Range: NA

Read/Write: R/W

Initialized Value: NA

Operational Settings: These events are NOT latched. They are dynamic. Use this register to read current or real-time status. It is recommended to read these events using the *Latched Status* register as the *Dynamic Status* register may capture a fleeting event. A purpose for this register is a sanity check to determine if a latched state still exists. See specific registers for function description and programming.

Dynamic Status																	
REGISTER	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
DYNAMIC STATUS	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BUILT IN SELF TEST (BIST) PASSED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CHANNEL CONFIGURED
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	GAP TIMEOUT OCCURED
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X=DON'T CARE
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
CHANNEL STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETx RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS HIGH Detect (rise)*
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS LOW Detect (fall)*
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS*

* Applies to SC1 only.

Latched Status

Function: Describes the status of 15 different events.

Type: binary word

Data Range: NA

Read/Write: R/W

Initialized Value: NA

Operational Settings: These events are latched and unlatched when read. See specific registers for function description and programming.

Latched Status																	
REGISTER	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
INTERRUPT STATUS (LATCHED)	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BUILT IN SELF TEST (BIST) PASSED
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CHANNEL CONFIGURED
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	GAP TIMEOUT OCCURED
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X=DON'T CARE
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
INTERRUPT STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & HDLC only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETx RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS HIGH Detect (rise)
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS LOW Detect (fall)

Note: The interrupts are cleared when a ("1") is written to the specific bit.

Interrupt Enable

Function: Provides for Interrupt Enabling.
Type: binary word
Data Range: NA
Read/Write: R/W
Initialized Value: NA
Operational Settings: Set bit High True to enable interrupts. Status will still be reported in status registers. See specific registers for function description and programming.

Interrupt Enable																
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	BUILT IN SELF TEST (BIST) PASSED
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CHANNEL CONFIGURED
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	GAP TIMEOUT OCCURED
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X=DON'T CARE
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETx RECEIVED
0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS HIGH Detect (rise)
0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS LOW Detect (fall)
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CTS

Set Edge/Level Interrupt

Function: Used to set interrupt detection types.
Type: unsigned integer
Data Range: 0x0000 0000 to 0xFFFFFFFF
Read/Write: R/W
Initialized Value: NA
Operational Settings: Set bit High True to enable level triggering. Set bit Low to enable rising edge triggering.

Set Edge/Level Interrupt																	
REGISTER	**D31**	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**FUNCTION**
EDGE/LEVEL - HI	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
REGISTER	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**FUNCTION**
EDGE/LEVEL - LO	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Function Register Map

0x1010	Rx Buffer Ch. 1	R
0x1014	Rx Buffer Ch. 2	R
0x1018	Rx Buffer Ch. 3	R
0x101C	Rx Buffer Ch. 4	R

0x1000	Tx Buffer Ch. 1	W
0x1004	Tx Buffer Ch. 2	W
0x1008	Tx Buffer Ch. 3	W
0x100C	Tx Buffer Ch. 4	W

0x1020	Number Of Words Tx Buffer Ch. 1	R
0x1024	Number Of Words Tx Buffer Ch. 2	R
0x1028	Number Of Words Tx Buffer Ch. 3	R
0x102C	Number Of Words Tx Buffer Ch. 4	R

0x1030	Number Of Words Rx Buffer Ch. 1	R
0x1034	Number Of Words Rx Buffer Ch. 2	R
0x1038	Number Of Words Rx Buffer Ch. 3	R
0x103C	Number Of Words Rx Buffer Ch. 4	R

0x1040	Protocol Ch. 1	R/W
0x1044	Protocol Ch. 2	R/W
0x1048	Protocol Ch. 3	R/W
0x104C	Protocol Ch. 4	R/W

0x1050	Clock Mode Ch. 1	R/W
0x1054	Clock Mode Ch. 2	R/W
0x1058	Clock Mode Ch. 3	R/W
0x105C	Clock Mode Ch. 4	R/W

0x1060	Interface Levels Ch. 1	R/W
0x1064	Interface Levels Ch. 2	R/W
0x1068	Interface Levels Ch. 3	R/W
0x106C	Interface Levels Ch. 4	R/W

0x1070	Tx-Rx Configuration Ch. 1	R/W
0x1074	Tx-Rx Configuration Ch. 2	R/W
0x1078	Tx-Rx Configuration Ch. 3	R/W
0x107C	Tx-Rx Configuration Ch. 4	R/W

0x1080	Control Ch. 1	R/W
0x1084	Control Ch. 2	R/W
0x1088	Control Ch. 3	R/W
0x108C	Control Ch. 4	R/W

0x1100	HDLC Rx Address/Sync Char Ch. 1	R/W
0x1104	HDLC Rx Address/Sync Char Ch. 2	R/W
0x1108	HDLC Rx Address/Sync Char Ch. 3	R/W
0x110C	HDLC Rx Address/Sync Char Ch. 4	R/W

0x1090	Data Configuration Ch. 1	R/W
0x1094	Data Configuration Ch. 2	R/W
0x1098	Data Configuration Ch. 3	R/W
0x109C	Data Configuration Ch. 4	R/W

0x1110	HDLC Tx Address/Sync Char Ch. 1	R/W
0x1114	HDLC Tx Address/Sync Char Ch. 2	R/W
0x1118	HDLC Tx Address/Sync Char Ch. 3	R/W
0x111C	HDLC Tx Address/Sync Char Ch. 4	R/W

0x10A0	Baud Rate Ch. 1	R/W
0x10A4	Baud Rate Ch. 2	R/W
0x10A8	Baud Rate Ch. 3	R/W
0x10AC	Baud Rate Ch. 4	R/W

0x1120	XON Character Ch. 1	R/W
0x1124	XON Character Ch. 2	R/W
0x1128	XON Character Ch. 3	R/W
0x112C	XON Character Ch. 4	R/W

0x10B0	Preamble Ch. 1	R/W
0x10B4	Preamble Ch. 2	R/W
0x10B8	Preamble Ch. 3	R/W
0x10BC	Preamble Ch. 4	R/W

0x1130	XOFF Character Ch. 1	R/W
0x1134	XOFF Character Ch. 2	R/W
0x1138	XOFF Character Ch. 3	R/W
0x113C	XOFF Character Ch. 4	R/W

0x10C0	Tx Buffer Almost Empty Ch. 1	R/W
0x10C4	Tx Buffer Almost Empty Ch. 2	R/W
0x10C8	Tx Buffer Almost Empty Ch. 3	R/W
0x10CC	Tx Buffer Almost Empty Ch. 4	R/W

0x1140	Termination Character Ch. 1	R/W
0x1144	Termination Character Ch. 2	R/W
0x1148	Termination Character Ch. 3	R/W
0x114C	Termination Character Ch. 4	R/W

0x10D0	Rx Buffer Almost Full Ch. 1	R/W
0x10D4	Rx Buffer Almost Full Ch. 2	R/W
0x10D8	Rx Buffer Almost Full Ch. 3	R/W
0x10DC	Rx Buffer Almost Full Ch. 4	R/W

0x10E0	Rx Buffer High Watermark Ch. 1	R/W
0x10E4	Rx Buffer High Watermark Ch. 2	R/W
0x10E8	Rx Buffer High Watermark Ch. 3	R/W
0x10EC	Rx Buffer High Watermark Ch. 4	R/W

0x10F0	Rx Buffer Low Watermark Ch. 1	R/W
0x10F4	Rx Buffer Low Watermark Ch. 2	R/W
0x10F8	Rx Buffer Low Watermark Ch. 3	R/W
0x10FC	Rx Buffer Low Watermark Ch. 4	R/W

0x1150	Time Out Value Ch. 1	R/W
0x1154	Time Out Value Ch. 2	R/W
0x1158	Time Out Value Ch. 3	R/W
0x115C	Time Out Value Ch. 4	R/W

0x1160	FIFO Status Ch. 1	R
0x1164	FIFO Status Ch. 2	R
0x1168	FIFO Status Ch. 3	R
0x116C	FIFO Status Ch. 4	R

BIT

0x0800	Dynamic Status	R
0x0804	Latched Status	R/W
0x0808	Interrupt Enable	R/W
0x080C	Set Edge/Level Interrupt	R/W

Status

0x0810	Dynamic Status Ch. 1	R
0x0814	Latched Status Ch. 1	R/W
0x0818	Interrupt Enable Ch. 1	R/W
0x081C	Set Edge/Level Interrupt Ch. 1	R/W

0x0820	Dynamic Status Ch. 2	R
0x0824	Latched Status Ch. 2	R/W
0x0828	Interrupt Enable Ch. 2	R/W
0x082C	Set Edge/Level Interrupt Ch. 2	R/W

0x0830	Dynamic Status Ch. 3	R
0x0834	Latched Status Ch. 3	R/W
0x0838	Interrupt Enable Ch.3	R/W
0x083C	Set Edge/Level Interrupt Ch. 3	R/W

0x0840	Dynamic Status Ch. 4	R
0x0844	Latched Status Ch. 4	R/W
0x0848	Interrupt Enable Ch. 4	R/W
0x084C	Set Edge/Level Interrupt Ch. 4	R/W

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